Improving Receive Sensitivity of the CPX Bus

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Acknowledgements

My Parents for supporting and guiding me throughout my life.

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The PolySat Team for designing and building an object currently orbiting our small home. The EE Team kept the irons hot, Team Software kept me awake during late nights in the lab, the ADC Team kept the spreadsheets flowing, and everyone had a good time.

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1 Introduction

Upon the successful launch of the CP2 and CP3 spacecraft in April 2007, the PolySat team immediately noticed a problem with the spacecraft's uplink margin. While the Cal Poly Earth Station could hear the satellites just fine, the satellites could not hear the earth station very well. It appears that the uplink problem relates to poor satellite receive sensitivity; however, as recent tests done at SRI International show, pass-dependent factors such as the orientation of the spacecraft might affect the link margin more than receive sensitivity.

Derek Huerta designed and built the communication subsystem for both satellites as part of his Masters Thesis in Spring 2006[1]. If everything went according to plan, CP2 would launch first and verify the entire satellite, including the communications subsystem. PolySat project members, who built the satellite, would fix the circuit before the next launch if it performed poorly in orbit. However, due to several delays and a launch failure[2], we made no improvements to the communications subsystem from CP2 to CP3.

This Senior Project will try and correct this situation. Scheduled to launch in October 2008, CP6 must function as well as possible, requiring an improved communications subsystem. To increase the uplink margin of the link, I will add a low-noise amplifier (LNA) and a high-pass filter (HPF) just before the CC1000 receiver. The satellite's Front Panel already contains a low-pass filter (LPF).

1.1 CubeSat Project Background

The CubeSat standard started as a joint project between Stanford University and Cal Poly State University in 1999[3]. Stanford Professor Bob Twiggs and Cal Poly Professor Dr. Jordi Puig-Suari imagined multiple 10 cm cubes in a jack-in-the-box type launcher after the experiences building and deploying picosatellites from the Orbiting Picosatellite Automated Launcher(OPAL).

OPAL, the second student satellite from Stanford University, contained six picosatellites in four custom-designed launch tubes[4]. Each launch tube measured 7.5x2.5 cm at the opening and stretched 20 cm into the satellite. One long picosatellite could fill one launch tube, or multiple picosatellites could pack together in the same space. Two of the launch tubes aboard OPAL had one satellite each, and the other launch tubes contained two satellites each. Each tube deployed with a separate signal from the main processor.

These picosatellites performed various missions. Two of the picosatellites, from Santa Clara University's Artemis Project, contained VLF receivers to study thunderstorms. Another from Santa Clara University contained a simple beacon to verify picosatellites could be heard from space. The Aerospace Corporation built two picosatellites that tested a 900 MHz transceiver, and connected them with a 10 meter tether. A group of amateur radio enthusiasts from the Washington D.C. area built the final picosatellite, called STENSAT. It contained a half-watt Mode J transponder[5].

The OPAL tube launcher design was the basis for the Poly Picosatellite Orbital Deployer, or P-POD[6]. Each P-POD can accommodate three 10x10x10 cm cubesats, or any combination of satellites that add up to 30 cm. The maximum mass for a single cubesat is 1 kg, derived from the equivalent volume of water.

Here at Cal Poly, the CubeSat Project designs, tests, and builds the P-POD. Two

Figure 1: OPAL. The deployment doors can be seen in the front.

versions of the P-POD have successfully flown; the Mark I aboard the Eurokot launch vehicle from Plesetsk Cosmodrome, Russia, and the Mark II aboard the Dnepr launch vehicle (SS-18) from the Baikonur Cosmodrome, Russia, and the Minotaur vehicle out of Wallops Island, Virginia. The Mark III will fly on the next Minotaur launch and on the next two Falcon launches from Kwajalein Atoll.

The CubeSat Project also performs integration and testing services for the launches they coordinate. This includes placing the cubesats in the P-POD, qualification vibration tests, shipping to the launch site, and integration of the P-POD onto the rocket. In addition to integration services, universities that do not have their own vibe or thermo-vac facilities may bring their satellites to Cal Poly for preliminary testing.

1.2 Cal Poly CubeSats

In addition to the launch services performed by the CubeSat Project, Cal Poly also builds satellites under the PolySat name. These two projects coexist peacefully in the same lab in the Advanced Technologies Laboratory in Building 007 on the Cal Poly campus.

The PolySat Project comprises of a multidisciplinary group of undergraduate and graduate students. It originally started as a joint project between Cuesta College and Cal Poly. Students at both institutions worked together to build the first CubeSat, naming it CP1. When key project students at Cuesta College transferred to Cal Poly, building of the satellites also moved entirely to Cal Poly.

1.2.1 CP1

The primary purpose of CP1, started in 2000, included the education of the next generation of satellite engineers. It also showed that a small, dedicated group of undergraduate and graduate students could build a picosatellite using cheap commercial off-the-shelf parts. No space-qualified hardware was used in construction of the satellite because of the costs involved. The payload included a sun sensor from Optical Energy Technologies. CP1 also

Figure 2: CP1 Flight 1.

experimented with using a cheap transceiver and DTMF modulation scheme to transfer basic telemetry and sun sensor data back to the ground[7].

The main processor of this satellite consisted of a Netmedia BX-24, essentially a common BASIC Stamp with more memory (both volatile and nonvolatile) and more I/O pins. The software, written in BASIC, consumed 73 kB of memory. Programming the satellite required it heated with a heat gun to speed up the clock.

The communication subsystem comprised of two modified Alinco DJ-C4 transceivers. Stripped of their cases, the radios mounted directly to the structure on either side of the satellite. Other modifications include removing the keypad/LCD assembly, li-ion battery, audio jacks, non-removable antenna, and output matching network. Ribbon cable, soldered directly between the modified Alinco radios and Command and Data Handling (C&DH) printed circuit board (PCB) allowed the BASIC Stamp to control the transceivers and RF switch[8]. The entire satellite did not contain any connectors, one feature that increased reliablility of the inter-board connections but required a lot of time and effort. The CP2 team did not use this connector-less design because of the pain it caused the CP1 team.

A separate RF Switch PCB, controlled by the main processor, connected both Alinco radios to the single antenna. This board also provided the necessary balun and matching network required for the balanced 50Ω to dipole impedance conversion.

1.2.2 CP2

Cal Poly's second satellite, CP2, started directly after the CP1 team finished. It continued the tradition of faster, cheaper, better. The entire satellite "bus" was redesigned for CP2, incorporating all the "lessons learned" from CP1. A satellite "bus" contains all the subsystems of the satellite, including power generation and storage, communications, command and data handling, and structure, except the payload. This allows future satellites to easily add a new payload (such as a camera) to a proven satellite design, reducing the risk by using flight-tested hardware and software.

In total, we built five CP2 satellites: TestSat, BenchSat, CP2 Flight 1, CP2 Flight 2, and another show-and-tell satellite:

- TestSat presently lives in pieces scattered about the lab. Not much of this satellite

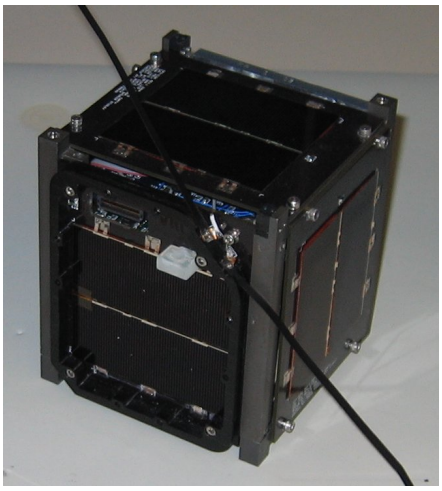


Figure 3: CP2 Flight 2. Blue wire-mods are visible on the C&DH board.

is left.

- BenchSat currently functions as our Engineering Unit. Before we send new commands to the satellite in space, we test them on this Engineering Unit to ensure that the command will not destroy the satellite. There are several commands that will render the satellite inoperable. We also use this satellite as a show-and-tell model.
- CP2 Flight 1 flew on the Dnepr Launch 1 flight. This launch failed[2].
- CP2 Flight 2, manifested as CP4, flew on the Dnepr Launch 2 flight. Originally our Engineering Unit, we upgraded it after the failure in case we wanted to launch CP2 again. Object 31132 in the NORAD database.

For the purposes of this project, I will refer to this satellite (and all its variants) as CP2. However, the official launch manifest refers to this satellite as CP4, as does the rest of the world. This confusion stems from the original CP4 satellite, which contained a CPX bus and deorbit experiment. When Dnepr 1 failed, we decided to re-fly CP2 instead. The Russian government would not let us change the launch manifest to reflect a different satellite, so we just renamed the satellite to CP4 to appease the bureaucrats.

The whole CP2 satellite, from conception to finished flight build, took one and a half years[9]. This is an incredibly short time, considering that almost none of the CP1 team members stayed on the project for the CP2 effort.

CP2 included some interesting design features[10]. Dual-junction solar cells (about 25% efficient) provide power for the spacecraft, charging two 2100 mAh lithium-ion cell phone batteries. Magnetorqueres, embedded in the middle three layers of the side-panel PCBs, allow the spacecraft to torque against the earth's magnetic field to point the spacecraft. The structure is comprised of milled 6061 aluminum, anodized for electrical insulation and to prevent cold welding to the P-POD before deployment.

After comparing different data bus technologies, such as CAN-bus and 1-wire, the team settled on the Inter-Integrated Circuit bus (I^2C), a low-speed motherboard bus developed by Philips Electronics. This bus snakes its way through the entire satellite, connecting all the different subsystems to the Command and Data Handling (C&DH) microcontroller via a MUX.

CP2 failed in orbit after approximately 3 months. While it is unclear why the satellite failed, several theories suggest a failure of the I^2C bus on the satellite. The CC1000 transceivers and comm PIC processors still function, but the C&DH processor appears dead. However, the C&DH still switches the transceivers every five minutes, so we speculate that some rogue device continuously transmits bad data on the I^2C bus.

Even though the satellite failed, it still responds to a limited set of commands, commands that do not need the C&DH processor to fulfill. Between CP3 passes, PolySat team members still try to contact CP2 and succeed on most attempts.

1.2.3 CP3

Our third satellite incrementally improves on the CP2 bus, introducing several bus improvements. The new payload contains two cameras, but due to bus contention issues, only one camera works. Many of the uplink commands have been rewritten in software, and perform more robustly than before.

CP3 contains essentially the same C&DH and Power boards as CP2, with minor incremental updates for obsolete parts. Replaced parts include the real-time clock and both battery monitors.

As with CP2, we built several CP3 satellites:

- TestSat presently lives in the lab. It doesn't have any side panels. The software team uses this satellite to develop the software for the satellite.
- BenchSat also lives on the Software bench in the lab. This satellite is fully complete.
- CP3 Flight 1 orbits earth, propelled into space on the Dnepr Launch 2 flight. Object 31129 in the NORAD database.
- CP3 Flight 2 will launch on the next Minotaur rocket with three other CubeSats and TacSat-3 as the primary.

This satellite launched, along with CP2, on the Dnepr 2 launch from Baikonur Cosmodrome in Kazakhstan. For the first two months we did not hear from it at all. Watching the cluster of satellites spread out over time, we sequentially tracked all the objects from the launch, wondering if some of the satellites were mislabeled. Our hunch turned out correct, and Justin Foley made contact with CP3 on June 16, 2007 (Graduation Day), using the Libertad-1 Keplerian elements. Appendix A shows on-orbit data collected from this spacecraft.

1.2.4 CP4

On orbit name for CP2. We used the CP4 name because the Russians wanted a satellite named "CP4", and changing the satellite's name is easier than changing the launch manifest.

1.2.5 CP5

Not yet scheduled for launch, this satellite's payload consists of a deployment experiment. It will use the next iteration of the standard CPX bus, with the payload taking up the same space as the cameras on CP3.

1.2.6 CP6

Our third satellite, scheduled for launch in October 2008, contains slight hardware and major software modifications to our CP3 satellite. The two hardware modifications include adding a low noise amplifier to the receiver (detailed in this Senior Project), and adding tri-state buffers between the cameras and the payload processor.

Since both cameras reside on the same data bus, and when one camera is sending data to the processor, voltage is present on the output lines of the other camera. While this voltage is only around 3 volts, we suspect that any voltage on the output pins destroys the sensitive CMOS imager. The tri-state buffers reside on the camera data bus between the processor and cameras and allow the payload processor to select only one camera to communicate with, keeping the input pins of the other image in a high-impedance state.

Software modifications for this satellite include increasing the reliability of the I^2C bus by adding a checksum value to the packets and collecting statistics on message errors[11]. Several uplink commands were re-written, allowing the sensor snapshot circular buffer to pause until the spacecraft is over a ground station.

1.3 Scope of Project

In order to increase the sensitivity of the satellite, I will add a low-noise (LNA) to the CPX Bus. The "CPX Bus" refers to the next version of satellite containing all subsystems (power, structure, data storage, communications, etc) of our cubesat except the payload. Figure 4 shows the entire communication subsystem, and Figure 5 shows the individual components of my Senior Project. As one can see, the scope of this project mostly encompasses matching the different devices to the 50Ω characteristic impedance of the microstrip on the 6-layer FR4 PCB.

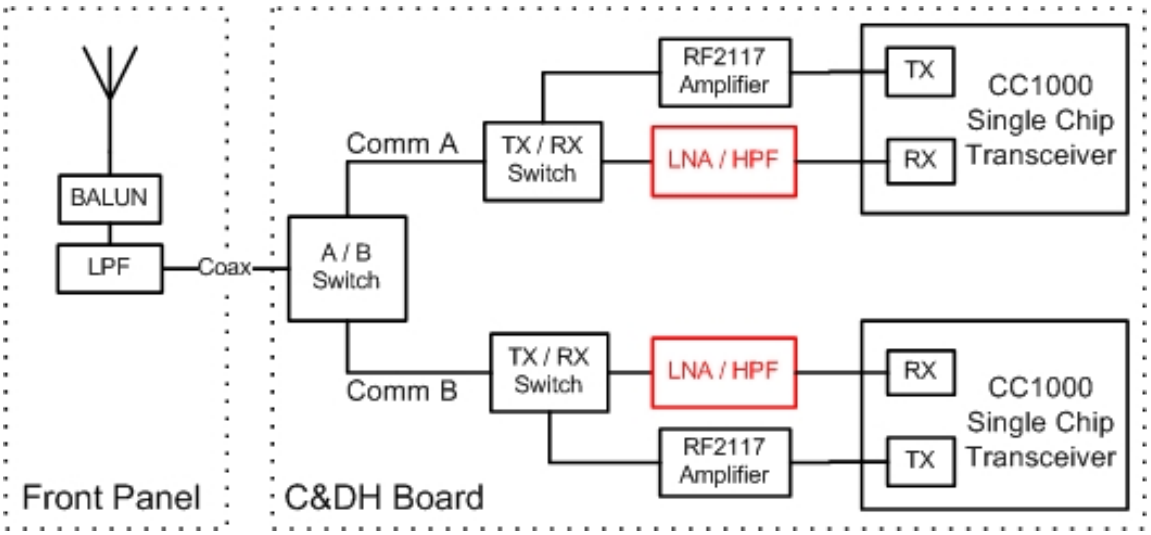


Figure 4: Block diagram of the satellite communications subsystem. Components not shown include the Comm A and Comm B processors, which control the A/B and TX/RX switches, RF2117 start-up sequence, and CC1000 single chip transceivers. This senior project resides within the LNA/HPF block, see Figure 5.

To make the matching process easier, I will purchase a development kit for the LNA. Based on the development kit, I will incorporate a rough matching network into the layout for the Command and Data Handling (C&DH) boards. This ensures the boards will not need fabrication again once I find the final matching network values.

Once I optimally match the LNA to the rest of the circuit, I will test the receive sensitivity. We never thoroughly tested the receive sensitivity of the original circuit, so the receive sensitivity of the old boards will be tested and compared to the new circuit. I will use the RF lab in Building 20 for this testing.

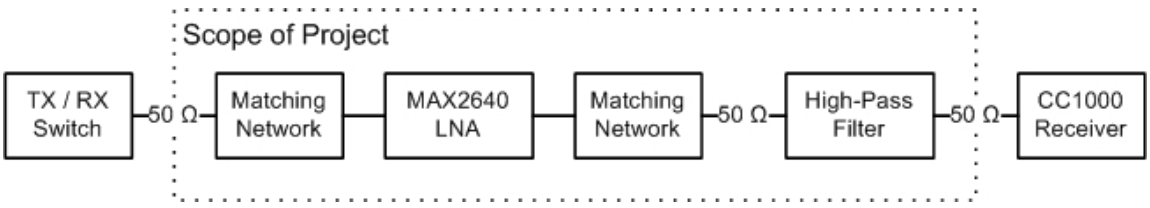


Figure 5: Scope of this senior project.

2 Measuring LNA Impedance

While the input and output impedance measurements are in the datasheet in rough tabular form, I felt it necessary to verify their measurements. During this measuring process, I can also measure the input and output impedances at different input voltages and temperatures. Table 1 shows the scattering parameters from the datasheet.

Table 1: Typical MAX2640 scattering parameters at 400 MHz, $V_{CC} = +3V, T_A = +25℃$, from the Maxim datasheet.

Parameter	**Magnitude**	**Phase**	**Comment**
S11	0.907	-35°	Input impedance
S21	4.62	109.1°	Forward gain
S12	0.001	13.5°	Reverse gain
S22	0.302	108.4°	Output impedance

Since the Network Analyzer measures S-parameters at the point where calibration occurred, it is necessary to extend the reference plane to account for the test fixture leads. While the magnitude (distance from center of Smith chart) does not change with reference plane extension unless the coax is extremely lossy, the phase (angle around Smith chart) does, and this drastically affects the final matching circuit. Two ways to measure this reference plane extension include using the Network Analyzer and using a ruler.

2.1 TDR with Network Analyzer

The Anritsu Network Analyzer contains a lowpass Time-Domain Reflectometry (TDR) mode. The Network Analyzer sends a pulse out and looks for any reflections back into the source. Any discontinuities in the feed line and any terminations are clearly shown as bumps or curves on the plots. TDR is used extensively in locating broken or shorted cables over long distances (kilometers).

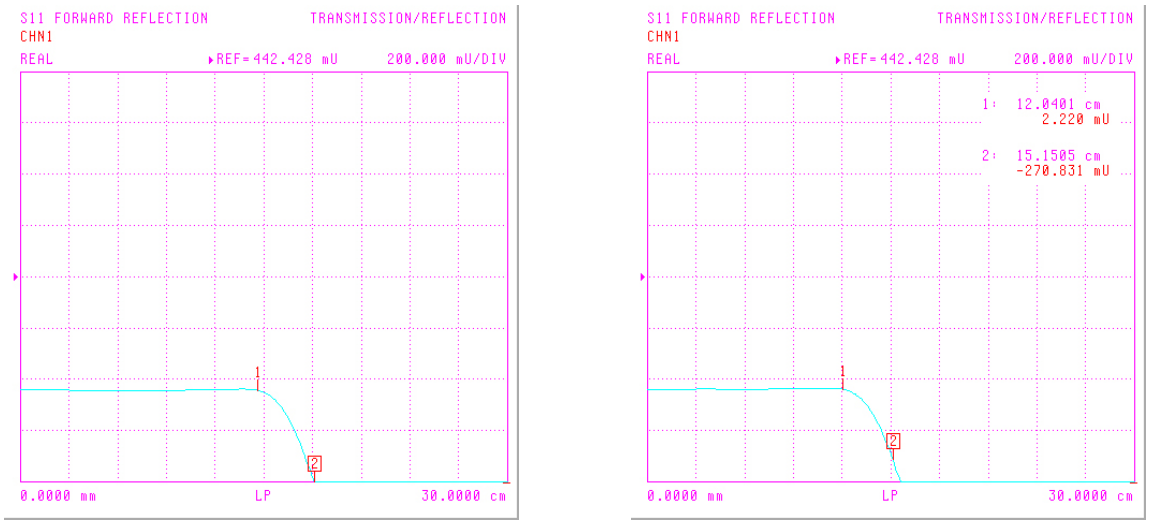
However, this Network Analyzer lacks the highly detailed TDR plot available from more specialized test equipment. The Network Analyzer can only generate frequencies, not functions, so it adds together many harmonically related frequencies to mathematically generate a step response. I calibrated the Network Analyzer in TDR mode from 10 MHz to 3 GHz, and shorted the ends of the semi-rigid coax to improve the reflections.

As one can see from Figure 6, the resolution of the TDR plots is not all that great. This limitation stems from the 3 GHz bandwidth of the Network Analyzer; a 20 GHz Network Analyzer TDR plot would be much sharper.

2.2 Physical Length Measurement

Another way to measure the distance of the test fixture leads includes using calipers to physically measure the distance.

Normally, the electrical length can be calculated from the physical length if one knows the speed of light in the coax, typically 2/3 the speed of light in air. However, the Network Analyzer is smart enough to calculate this electrical length if it knows the dielectric of the coaxial cable. I used the preset value of 2.6 for the teflon dielectric used in the semi-rigid coax.



(a) Input TDR (b) Output TDR

Figure 6: TDR measurement of the LNA input and output with the Network Analyzer. The plot rolls off at about 14 cm and 12 cm from the calibration point, indicating the end of the semi-rigid coax.

2.3 Building the Test Fixture R1

To easily measure the input and output impedance of the LNA, I built a test fixture using a small section of copper-clad printed circuit board (PCB) and semi-rigid coaxial cable. I placed the LNA chip on the PCB dead-bug style, bent the three ground pins back down to the ground plane, and soldered them down. I then positioned the semi-rigid coax near the input and output (see Figure 7 for chip pinout) and soldered the shield to the PCB. I left a small space between the center conductor and pin in case I fried the LNA and needed to replace it in the future.

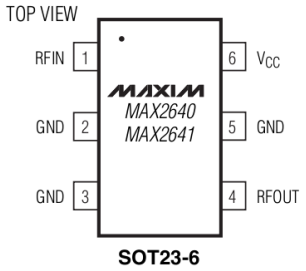


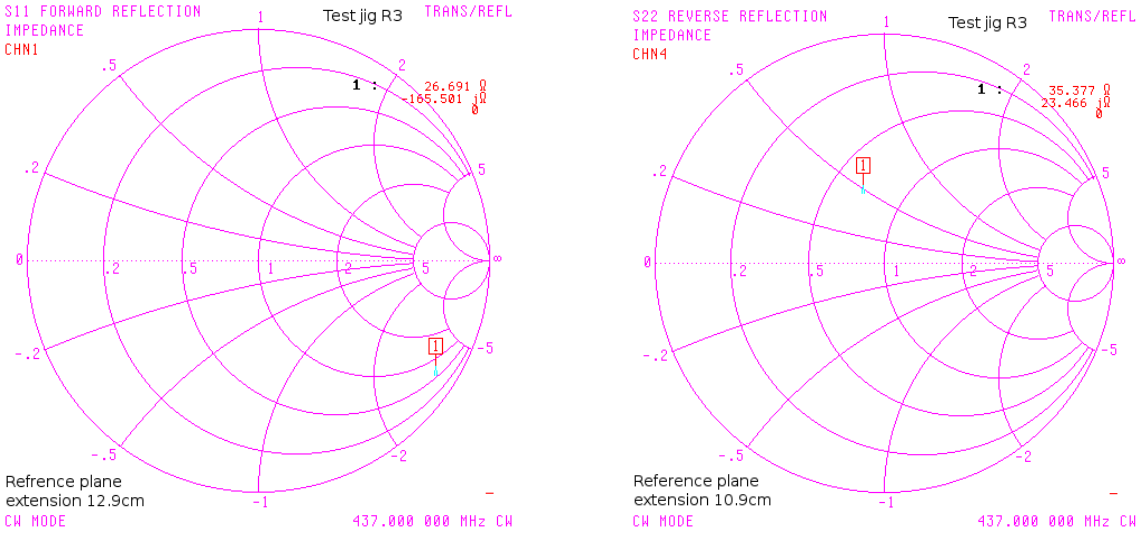
Figure 7: Pinout of MAX2640 LNA[12].

2.4 Results R1

I measured the input distance at 12.9 cm and the output distance at 10.9 cm. After extending the reference planes by these amounts, I measured the input impedance at 45.8-156j Ω and the output impedance at 34.4+21.4j Ω with an input of 3 volts at room temperature.

Figure 8: Oblique picture of the LNA test fixture. The 10µF bypass capacitor, at left, is bigger than the 1µF bypass capacitor. This chip is upside-down, so RF Input is from the top, and output is toward the bottom.

I also measured the effect of different voltage on the device input and output impedance. These results can be seen in Table 2. As one can see, the input impedance varies just a little and the output impedance is almost constant across the input voltage range. Results from measuring this test fixture are shown in Figure 9.



(a) S11 Input Impedance (b) S22 Output Impedance

Figure 9: Test Fixture R1 impedance, as measured with the Network Analyzer.

Table 2: Impedance as a function of input voltage.

Voltage (volts)	**Current (mA)**	**Impedance**	
		Input (Ω)	**Output (Ω)**
2.7	3.1	46.0 - 153j	34.5 + 21.4j
3	3.2	45.8 - 156j	34.4 + 21.4j
3.5	3.5	45.6 - 163j	34.4 + 21.4j
4	3.8	45.3 - 176j	34.3 + 21.5j
4.5	4.3	44.8 - 201j	34.2 + 21.5j
5	4.7	45.1 - 220j	34.2 + 21.5j
5.5	4.9	46.2 - 226j	34.1 + 21.5j

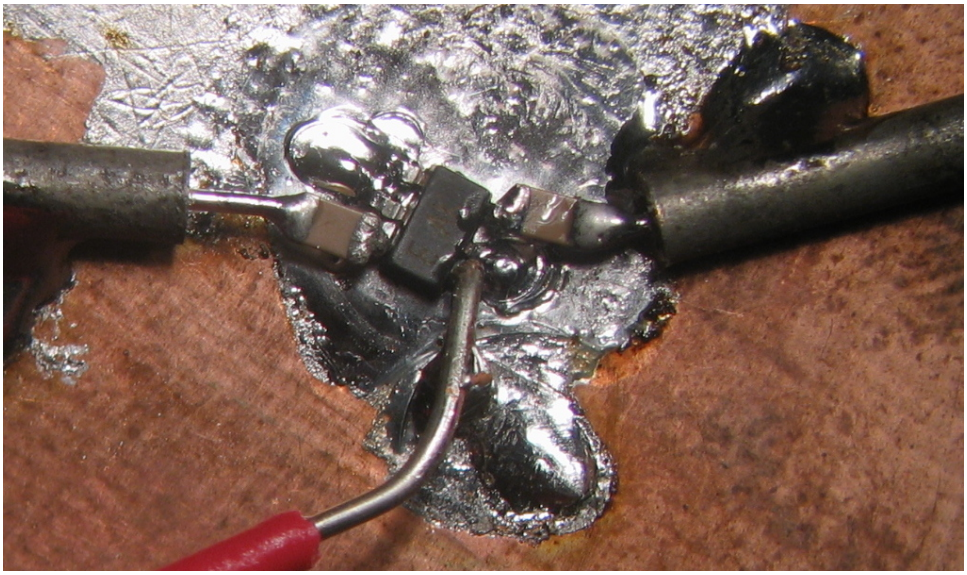


Figure 10: New test fixture with the 1000 pF DC blocking capacitors on the input and output. Input comes from the left, and output goes to the right. The two capacitors are suspended.

2.5 Building the Test Fixture R2

During the course of trying to match the low-noise amplfier to the board, I realized that the Network Analyzer was not AC coupled. Since the design of the LNA allows DC voltage to appear on the input and output pin, the Network Analyzer was shorting this voltage to ground, causing the LNA to not function properly. I then built another test fixture with 1000 pF capacitors between the Network Analyzer connections and the pins on the LNA. Figure 10 shows a picture of this new test fixture.

The 1000pF ceramic capacitors do not affect the operation of the LNA at all, they just provide a DC block. To calculate the resistance of the capacitors at 437 MHz, we use Equation 1. This shows that the resistance of the DC blocking capacitor is only 0.36 ohms, not significant enough to affect the circuit.

$$X_c = \frac{1}{(j * \omega * C)} = \frac{1}{(2\pi f * C)} = \frac{1}{(2\pi 437MHz * 1000pF)} = 0.36\Omega \quad (1)$$

2.6 Results R2

Figure 11 shows results from the second revision of the new test fixture with the 1000 pF capacitors. Notice that the input impedance changed dramatically but the output impedance did not. Also, the unmatched circuit also has around 10.5 dB of gain.

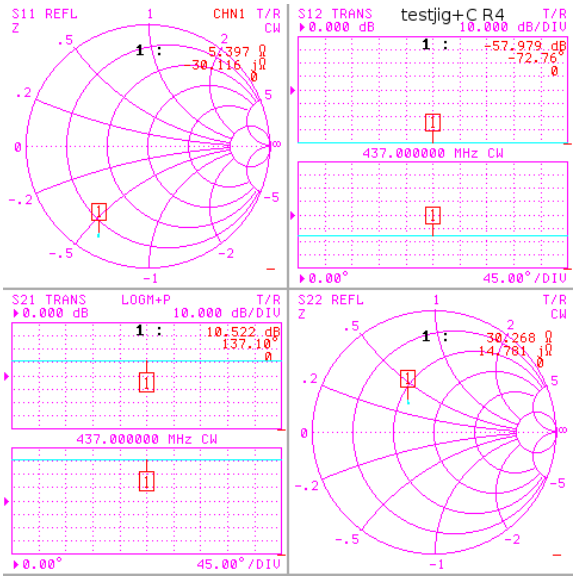


Figure 11: Scattering parameters as tested on the test jig with DC block capacitors.

3 Building the Matching Network

Now that we know the input and output impedances of the LNA, we can plot these values on a Smith chart to graphically solve the matching problem. A mathematical solution to matching is possible but much more difficult than using a Smith chart.

Invented by Philip Smith in 1939, the Smith chart allows engineers to solve complex equations for matching circuits and transmission lines using a simple graphical chart of normalized impedances and admittances. These normalized values are plotted on the chart, and the objective is to move along the circles to arrive at the center of the chart, which is the system impedance, usually 50Ω.

3.1 Equations

The objective for matching is to get to the center of the Smith chart. To travel around the Smith chart, one adds series or shunt elements to the circuit, working from the impedance of the chip to the center of the chart.

Most people prefer to use the standard Impedance (Z) Smith chart. However, I find it easier to use a ZY Smith chart, which plots normalized Impedance values in red and normalized Admittance values in blue. This allows me to find values without spinning the Smith chart 180°.

Use Equation 2 when travelling along the Impedance (red) Smith chart in a clockwise direction, adding series inductance to the circuit:

$$|X_L|_{normalized} = \frac{\omega * L}{Z_0} = \frac{2\pi f * L}{50} \tag{2}$$

When travelling along the Impedance (red) Smith chart in a counterclockwise direction, use Equation 3 to add series capacitance to the circuit:

$$|X_C|_{normalized} = \frac{1}{\omega * C * Z_0} = \frac{1}{2\pi f * C * 50} \tag{3}$$

Use Equation 4 when travelling clockwise along the Admittance (blue) Smith chart to add shunt capacitance:

$$|B_C|_{normalized} = \omega * C * Z_0 = 2\pi f * C * 50 \tag{4}$$

When travelling counterclockwise on the Admittance (blue) Smith chart, use Equation 5, adding shunt inductance:

$$|B_L|_{normalized} = \frac{Z_0}{\omega * L} = \frac{50}{2\pi f * L} \tag{5}$$

While these equations work well on paper, in reality they are usually used as starting points when building matching networks. As one can see in my many matching revisions, unknown board factors drastically affect the matching circuit. Use surface-mount prototyping kits to try different values of inductors and capacitors.

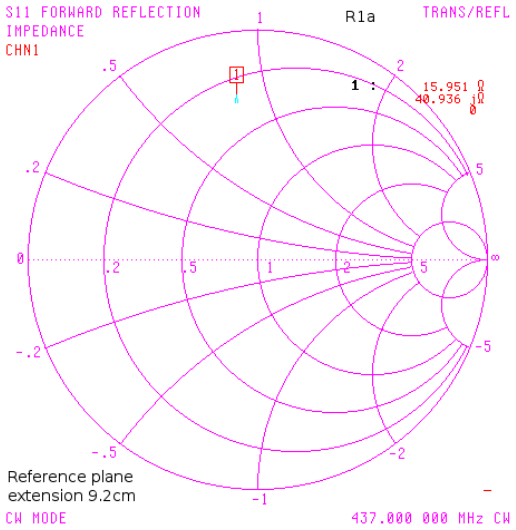
3.2 Revision R1

Using the input and output impedances I just measured on the test fixture, I proceeded to design a matching circuit using a Smith chart. As one can see from Figure 9, the input impedance lies almost on the R = 1 line, so matching this to the 50 ohms should be very straightforward.

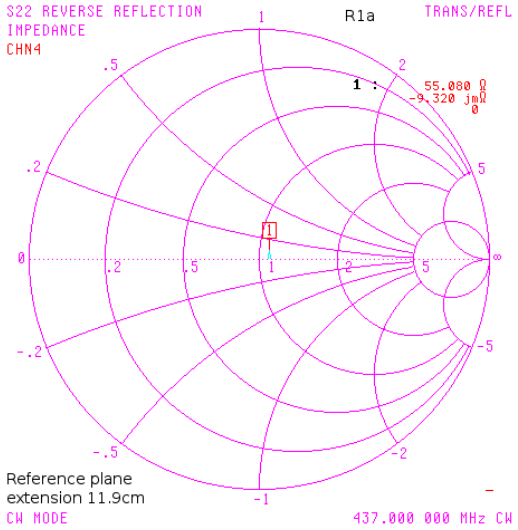
The MAX2640 requires a DC blocking capacitor on the input and output, meaning that the first device connected to the LNA input and output must either be part of the matching network (and must be a "series C" device on the Smith chart) or be a RF short at 437 MHz. To calculate a RF short, we can use the Equation 1. Using this equation, a capacitance of 1000 pF equals 0.36Ω of resistance at 437 MHz.

The TX/RX switch just before the input to the LNA also requires a DC blocking capacitor when positive control voltages are used, so a 1000 pF capacitor already exists on the board for this purpose. Therefore, I will not need to include a DC-block capacitor during matching, provided that a shunt inductor is not necessary.

For input matching, I used a 47 nH inductor only, resulting in an impedance of 10+24.3jΩ. For output matching, I used an 8 pF capacitor in series then a 12 nH inductor to ground, resulting in an impedance of 54+0.5jΩ. The output impedance is very close to the ideal value of 50Ω, so I will only focus on the input impedance matching for the rest of the revisions.



(a) S11 input impedance.



(b) S22 output impedance.

Figure 12: Iteration 1 results.

Just after testing, I realized that I had not cut the trace leading back to the HPF. I then cut the trace and re-measured the S22 parameters, Figure 13 shows the output impedance.

The difference between the two S22 parameters is the board capacitance. The difference, along the shunt capacitor line, is 0.6 units. Using Equation 4, we calculate the board capacitance at 12.2 pF along the 28.3 mm towards the high-pass filter. This equals about 4.3 pF per centimeter. During further testing, I decided to just solder the semi-rigid coax directly to the 0Ω resistor. This required the addition of a 4 pF capacitor to compensate

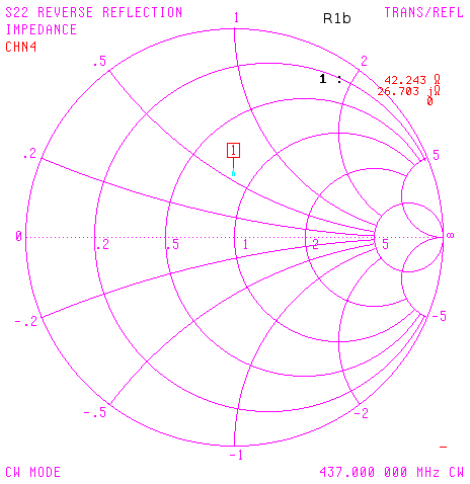


Figure 13: S22 results for iteration 1 with the trace cut.

for the missing trace.

3.3 Revisions RA through RN

While looking at the testing of Revision R1, I noticed that the current consumption of the LNA was very low, 0.8 mA, much lower than the nominal 3 mA. What could be causing the LNA to short out? I realized that the Network Analyzer was not AC coupled, shorting the input to the LNA. This may have been one factor why first revision did not match. Having essentially solved the output matching circuit, starting with revision RA I focused on the input matching network. The results of my matching can be seen in a tabular format in Table 3 and in a graphical format in Figure 14.

Table 3: Revisions RA through RN. Graphed on a Smith chart in Figure 14.

Iteration	**Series**	**Shunt**	**Results**	**Next Step**
A	47 nH	0	17 + 49j	Less inductance to get on Y = 1 line
B	22 nH	0	10.5 - 0.36j	Add shunt L to get to center
C	22 nH	82 nH	11.5 - 18j	Destroyed board; new board next revision
D	0 Ω	0	9 - 53j	Testing board; Need 0.66 series L = 12 nH
E	12 nH	0	11 - 37j	Need double the inductance to get to Y = 1
F	27 nH	0	16 - 5.8j	Too much added inductance
G	22 nH	0	13 - 18j	Good! Try adding shunt L
H	22 nH	120 nH	15 - 19j	Need more shunt L
I	22 nH	270 nH	16 - 12j	Biggest value inductor I have; Try using shunt C instead
J	47 nH	0	28 + 70j	Too much series L
K	33 nH	0	16 + 10j	Too little series L
L	39 nH	0	22 + 34j	Good! Try adding 1.0 shunt C = 7.3 pF
M	39 nH	9 pF	48 + 2.0j	Done with input. Add 4 pF to output
N	39 nH	9 pF	45 - 7.3j	Final matching

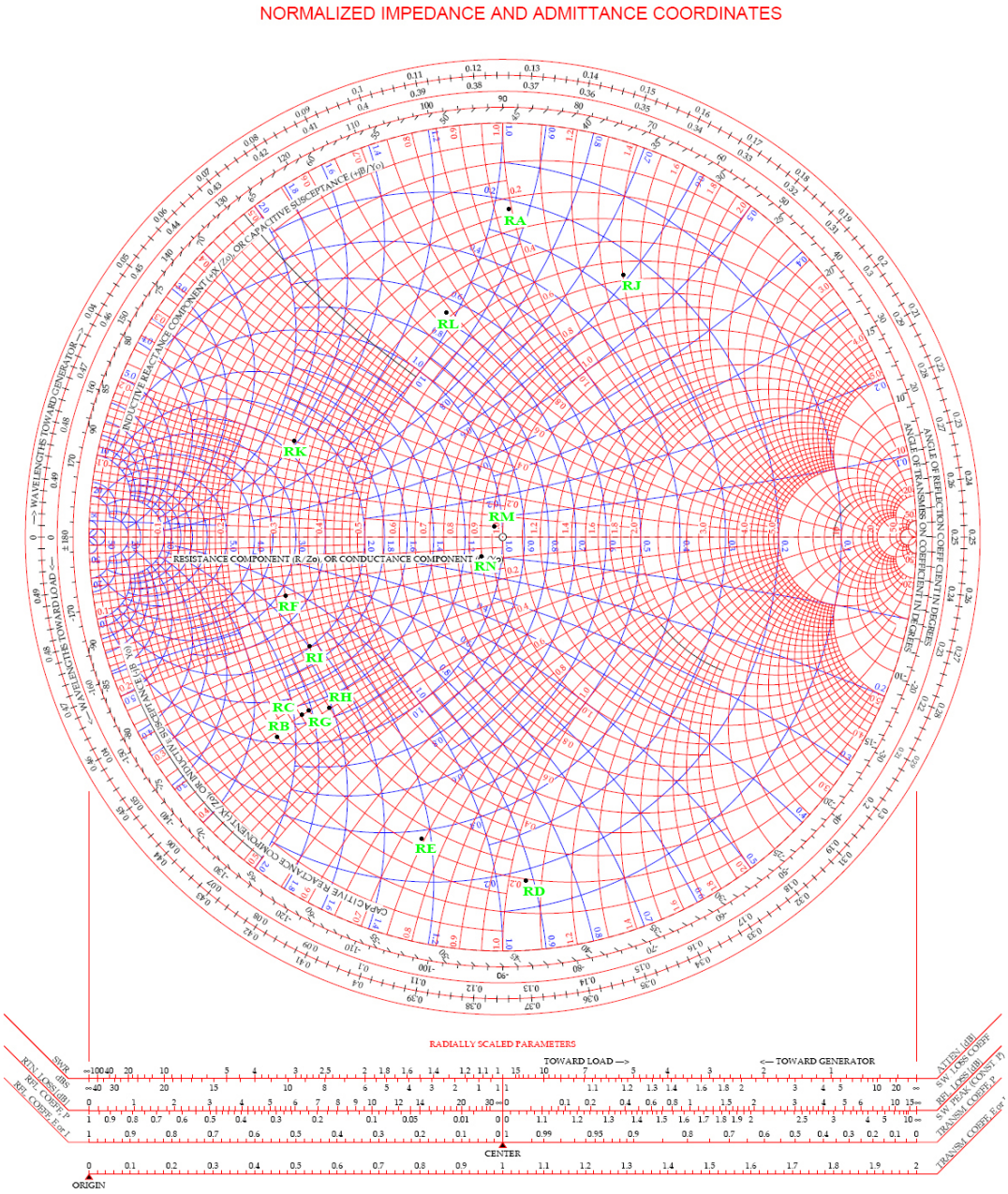


Figure 14: Smith chart for Revisions RA through RN. Used in conjunction with Table 3.

4 Final Circuit

The final matching circuit is identical to Revision RN for the input and Revision R1, with 4 pF capacitor, for the input. Figure 15 shows the S-parameter results of the final matching circuit, with 14.8 dB of gain and 43.7 dB of reverse isolation. Figure 27 shows a schematic of the final matching circuit.

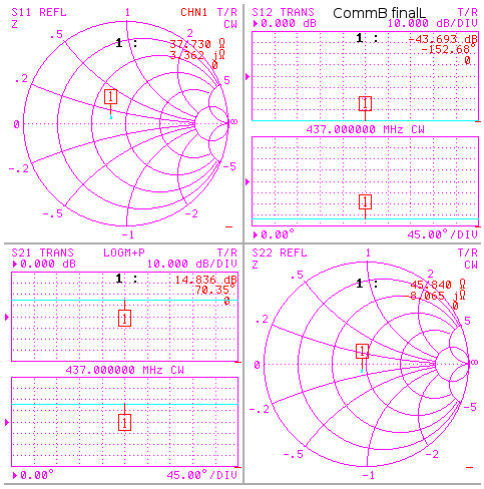


Figure 15: S-parameters for final matching circuit. Input impedance is 37.7+3.4jΩ, forward gain is 14.8 dB, reverse attenuation is 43.7 dB, and output impedance is 45.8-9.1jΩ.

Very few external components are required for the matching circuit. Table 4 lists the parts required to for matching, adding up to a total of 19 components. As one can see, the two LNAs cost $2.50, accounting for about half of the cost. The other capacitors, inductors, and resistors bring the total cost up to $5.167 per satellite.

Table 4: Parts list per satellite.

Qty	Description	Size	Ref Number	Supplier	Part Number	$ Each
2	LNA	SOT-23	U39, U38	Maxim IC	MAX2640AUT+	1.250
2	39nH ceramic	0603	L25, L24	DigiKey	334-1018-1-ND	0.563
2	12nH ceramic	0603	C136, C140	DigiKey	334-1012-1-ND	0.563
4	1000pF DC block	0805	C128, WM	DigiKey	PCC102BNCT-ND	0.043
2	9pF cap	0603	WM	DigiKey	PCC090CVCT-ND	0.033
2	8pF cap	0603	C135, C131	DigiKey	PCC080CVCT-ND	0.033
2	4pF cap	0603	C138, C141	DigiKey	PCC040CVCT-ND	0.033
3	0Ω resistor	0805	L26, L27, C127	DigiKey	311-0.0ADKR-ND	0.015
					Total:	**$5.167**

4.1 Noise Figure

Noise generated and amplified by the LNA affects the total circuit noise, decreasing the signal-to-noise ratio of the receiver circuit. The datasheet specifies the noise figure at 0.9

dB at 900 MHz, but the noise figure graphs do not extend less than 800 MHz. I measured the noise figure of the LNA on Comm B.

I performed noise figure measurements with a calibrated Anritsu NC364B noise source and the Network Analyzer. I used the EE480 lab manual[13] and the Anritsu Noise Figure application note[14] for testing procedures. The noise source works by rapidly switching between two known noise sources, a hot source and a cold source. The Network Analyzer then measures the difference between the two and calculates the noise figure.

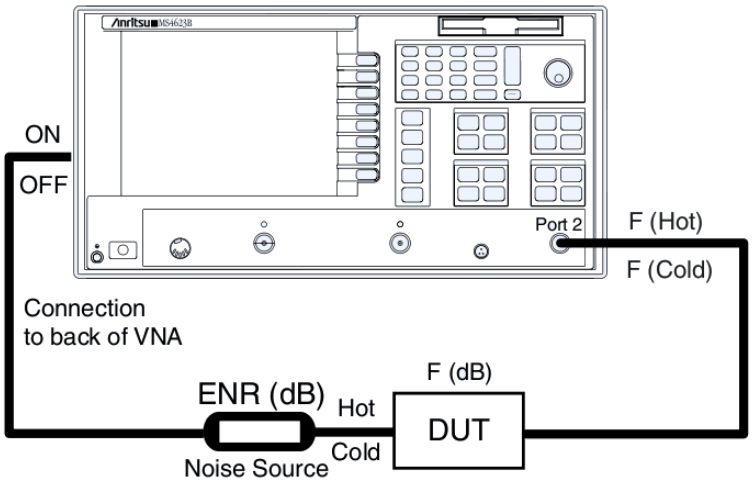


Figure 16: Noise figure measurement configuration. The noise source output connects to the input of the amplifier, and the output of the amplifier plugs into Port 2[14].

I used a noise source with 15 dB of Excess Noise Ratio (ENR). Due to the small noise figure I was trying to measure, a 6 dB ENR source would have allowed me a much more accurate measurement, but I did not have access to a 6 dB noise source. The noise figure measurement may be up to 0.5 dB off because the measured gain is about 0.5 dB off of what was measured with the Network Analyzer in Transmission/Reflection mode.

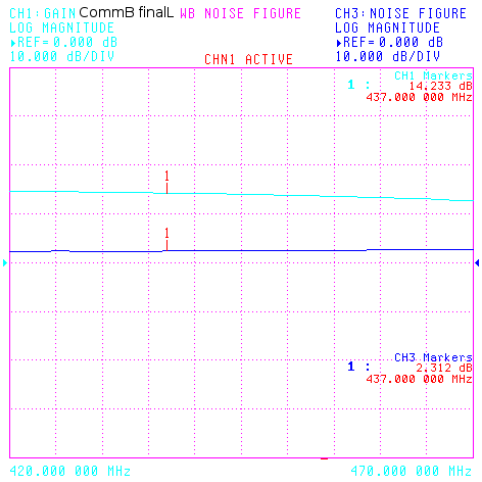


Figure 17: Noise measurement for Comm B. This shows the gain at 14.2 dB (channel 1 light blue) and the noise figure at 2.3 dB (channel 2 dark blue).

4.2 1 dB Compression Point

The 1 dB compression point specifies when the amplifier will start compressing the output signal with respect to the input signal. Distortion starts to occur at this point, so it is best not to exceed this point.

To measure the 1 dB compression point on the Network Analyzer, I used the procedures in the EE480 lab manual[13]. Set to a single frequency of 437 MHz, the Network Analyzer sweeps the input power from -45 to -20 dBm, then looks at the gain of the amplifier. The 1 dB compression point occurs where the gain rolls off by 1 dB.

Figure 18 shows the 1 dB compression point for this amplifier occurs at -24.9 dBm. The 1 dB compression point is measured off of the linear region of the amplifier, indicated by Marker 1. The data sheet specifies this value at -22 dBm at 900 MHz, so my measurements are very close given the huge frequency difference. As a bonus, the plot also shows input SWR at 1.3:1.

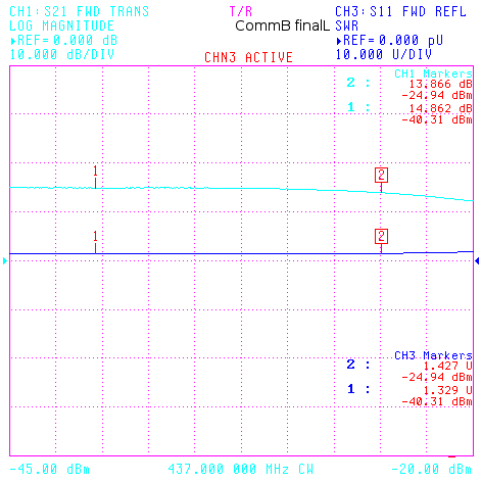


Figure 18: Light blue trace shows the 1 dB compression point measurement for Comm B at -24.9 dB. The 1 dB compression point is measured off of the linear region of the amplifier, denoted here by Marker 1. The dark blue trace shows the input SWR at 1.3:1.

4.3 Temperature Variation

As Figure 29 in Appendix A shows, the internal temperature of the spacecraft varies between -20℃ and +25℃. Therefore, I felt it necessary to look at the effects of temperature on the amplifier. I found that as the chip performed better at colder temperatures; the current consumption dropped by 0.8 mA and noise decreased by about 0.4 dB. Figures 19 and 20 show the actual experimental data.

For this thermal testing, I placed a standard C&DH board with leads in a sealed plastic bag, along with several desiccant bags to keep the moisture in the air from condensing onto the board and shorting the amplifier. Figure 21 shows the test configuration. I used a block of dry ice as the coolant, and used paper as insulation between the dry ice and the C&DH board. Even with the insulation, the temperature dropped so fast that I ended up taking pictures of the Network Analyzer and transcribing the data afterwards.

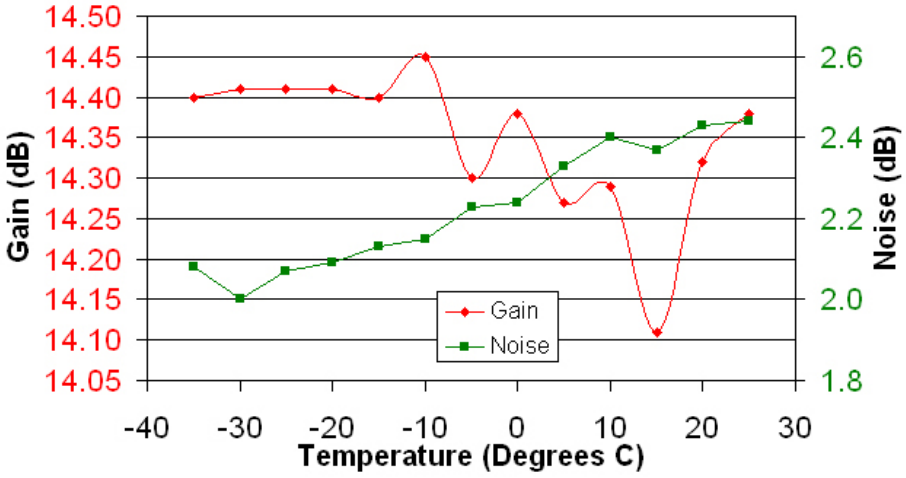


Figure 19: Temperature effects on noise and gain. The gain of the amplifier is less affected than the noise, which decreases from more than 2.4 dB to around 2.0 dB from room temperature to -35℃.

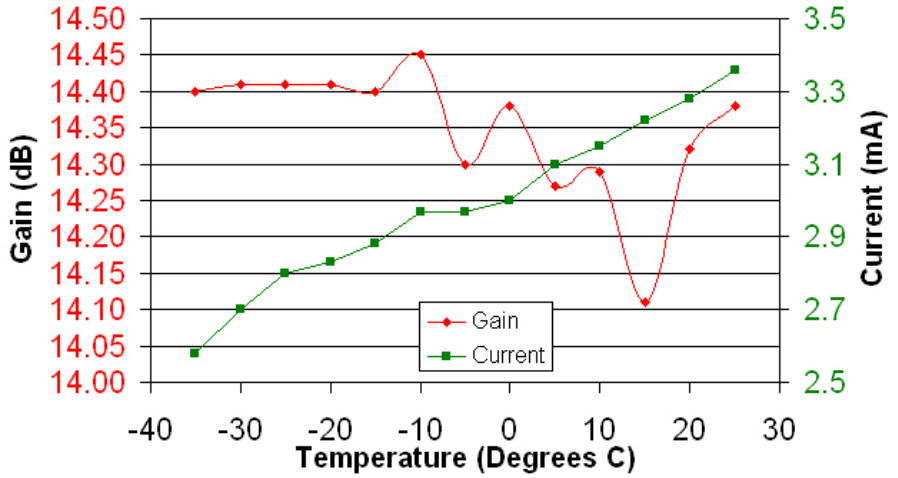


Figure 20: Temperature effects on current consumption and gain of the amplifier. The current drops from 3.4 mA at room temperature to less than 2.7 mA at -35℃. The chip voltage is 3 volts.

4.4 Filter Performance

A Coilcraft S3HP307 high-pass filter is located after the LNA just before the input to the receiver, and a Mini-Circuits LFCN-530 low-pass filter exists on the front panel next to the antenna. This project added the high-pass filter after the LNA to simulate a band-pass filter. To see what affect these two filters have on this circuit, I built a test fixture with both these filters in series to measure the passband response.

The results (Figure 23) from this test shows that the insertion loss of the two filters at 436 MHz is 0.98 dB. The 3 dB bandwidth is the difference between Markers 2 and 3, and is 389 MHz wide. This is a little too wide, indicating that the low-pass filter could be swapped for one with a lower cutoff frequency. The Mini-Circuits LFCN-490 filter has a 3

Figure 21: Set-up for the thermal testing. The desiccant bags on the right prevents condensation from shorting out the chip. The temperature probe is under the copper tape at the top.

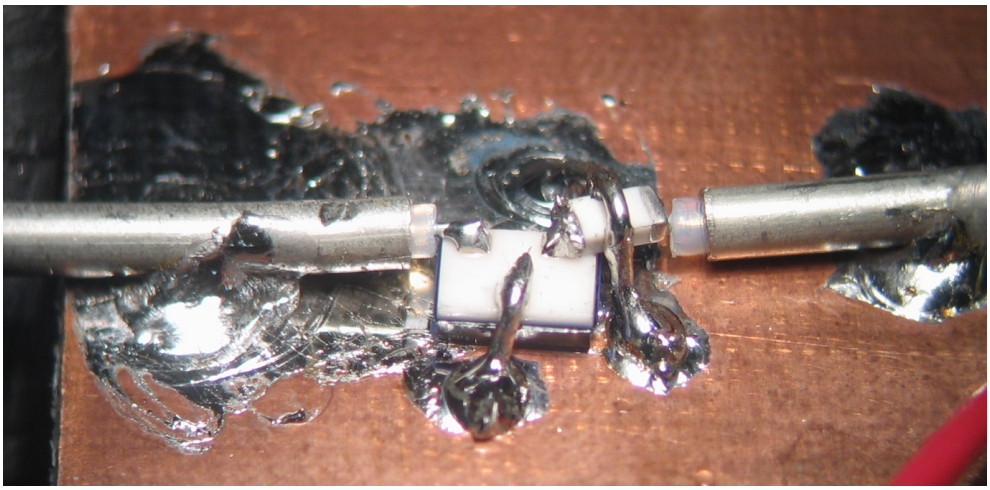


Figure 22: Test fixture for filters. The Coilcraft S3HP307 HPF is on the left side, and the Mini-Circuits LFCN-530 LPF is on the right side, with a grounding wire over the top.

dB cutoff frequency of 650 MHz instead of the approximate 700 MHz of our current filter, and would reduce the 3 dB bandwidth by about 50 MHz.

4.5 Powering the amplifer

During testing, I realized that the amplifier would be on when the high-power transmitter amplifier is on. This is a problem, as the absolute maximum input power to the LNA (from the datasheet) is +5 dBm, so I hoped that the RF switch isolation would be great enough to reduce the input signal far below this power level. Furthermore, less damage to the amplifier would occur if the input power never exceeded the 1 dB compression point of the amplifier (-24 dBm).

For a quick check, I looked at the isolation graph in the SW-425 data sheet in Ap-

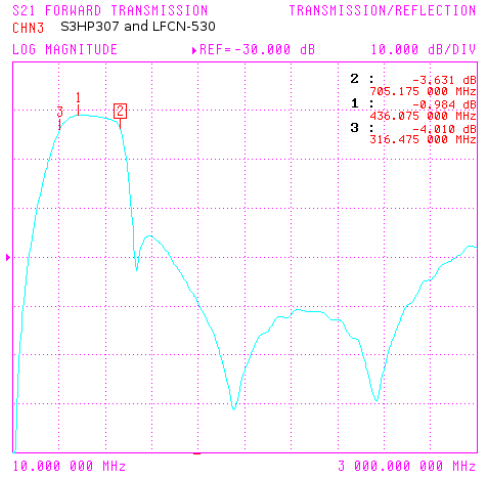


Figure 23: Passband for the combined low-pass and high-pass filters. Insertion loss is 0.98 dB with a 3 dB bandwidth of 389 MHz.

pendix B. The specified isolation is only about 27 dB. With around +30 dBm of transmitter power and 30 dB of switch isolation, approximately +3 dBm of power (2 mW) is present at the input of the amplifier. This is 27 dB more than 1 dB compression point and dangerously close to the +5 dBm absolute maximum input power, and may destroy the LNA.

To verify the datasheet and see how much power actually enters the LNA when the transmit amplifier was on, I built another test stand (Figure 24) for the RF switch. The switch also requires DC blocking on all inputs and outputs, so I included three 220 pF capacitors on the test fixture. For mechanical strain relief, I added 1 µF capacitors to the switching lines.

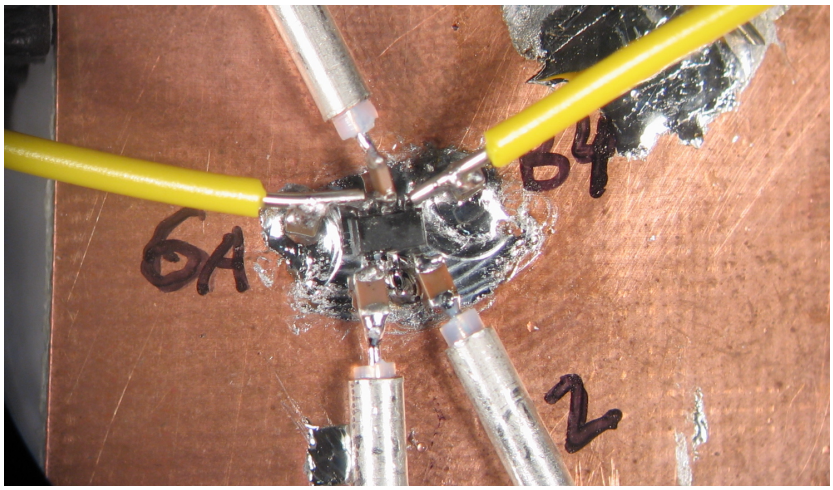


Figure 24: Test fixture for the SW-425 TX/RX RF switch. The common terminal (antenna) is at the top, and the two switch terminals (transmitter and receiver) are at the bottom. The 220 pF capacitors are for DC blocking, and the yellow leads are for the +3 volt switching. The 1 µF vertical capacitors on the switching lines are for mechanical strength.

The test procedure for measuring isolation includes the use of a Signal Generator, Spectrum Analyzer, and dummy load. I used +0 dBm of input power on RF1 and measured the output power on RF2 with the dummy load attached to the common pin RFC. Figure 25 shows the test setup.

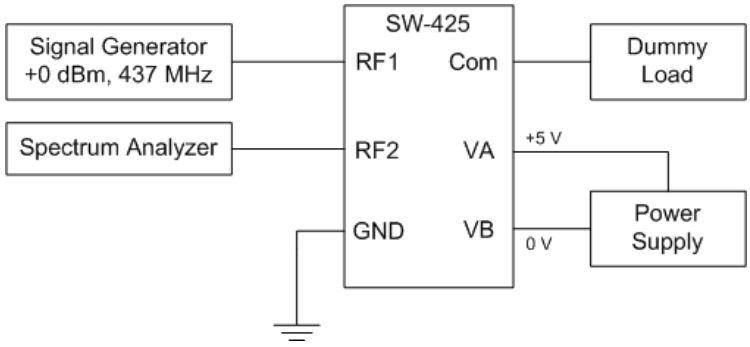


Figure 25: Block diagram for the RF switch isolation testing. Appendix B shows the truth table for the VA and VB input voltages.

Results showed that the switch has around 28.4 dB isolation between the two switched terminals, slightly more than the specification. This leaves us with around +2 dBm of input power to the LNA when the satellite is transmitting, very close to the +5 dBm maximum. Two solutions to this problem exist: assume everything will be OK because there is about 3 dB of margin, or somehow turn off the LNA when transmitting. I favor the second solution because it is easy to do, requiring only one wire modification and possibly an easy software change.

The favored solution includes turning the LNA off when transmitting. This could be easily accomplished by powering the LNA off of the SEL_RX control lines, which go high (up to +3 V) when receiving and low when transmitting. Power for this line comes from the communications PIC processor pin 36 (RC5/SDO), a standard digital I/O or SPI line capable of sourcing 25 mA. This pin, along with the SEL_TX lines, are bit-banged when the transceiver switches states from transmitting to receiving.

Unfortunately, any noise present in the PIC processor, such as crystal or switching noise, might also be present on this line and enter the LNA, although the filter capacitors might help a little with that. This extra filter capacitance might cause problems with switching the RF switch, as it might cause a high condition on both VA and VB pins for a very short while, putting the switch into an undefined state. Extensive timing testing is necessary before this option should be adopted. If problems arise, software can be modified to increase the switching time.

4.6 Matching Network Installation Procedure

Due to scheduling issues, PCB fabrication occurred long before the we knew the topology of the final matching network. Therefore, we made an educated guess about the quantity and placement of pads on the PCB, adding extras and hoping that we would not need more. As it turned out, the output matching network board layout had enough pads, but the input did not. Board modifications are necessary, and are outlined below.

4.6.1 Input

Refer to Figure 26 for a picture of the modifications.

1. Carefully remove Comm B TX/RX switch (U31) if populated. Discard.
2. Using a new sharp Xacto knife blade, carefully cut and remove 3 traces:
   - Between Comm A LNA (U39) pin 1 and L25, leaving 0.5 mm trace on the LNA side.
   - Between Comm B LNA (U38) pin 1 and L24.
   - Between Comm B TX/RX switch (U31) pin 3 and C127, leaving 0.5 mm trace on the switch side.
3. Scrape off the soldermask and silkscreen from the Comm B TX/RX switch (U31) pin 2 to the ground via nearby, and the two 0.5 mm trace stubs left in the previous step.
4. Install the two LNAs, being careful not to heat the chip too much.
5. Solder on the three 1000 pF DC block capacitors:
   - Between Comm A LNA (U39) pin 1 and nearby L25 pad.
   - Between Comm B LNA (U38) pin 1 and nearby L24 pad.
   - On C128.
6. Install L24 and L25, 39 nH inductors.
7. Mount the 9 pF shunt capacitors:
   - Between L25 and the ground pad of C130 (denoted by the larger trace going directly to a nearby via).
   - Between C127 and pin 2 of the Comm B TX/RX switch (U31). Do not solder the U31 side yet.
8. Install the Comm B TX/RX switch (U31). Solder all the pads, and connect pin 2 with the nearby 9 pF capacitor.
9. Solder the last remaining 1000 pF DC blocking capacitor between U31 pin 3 and C127, next to the 9 pF shunt capacitor. Ensure that no short exists between the switch pins.
10. Install a 0 Ω resistor on C127.

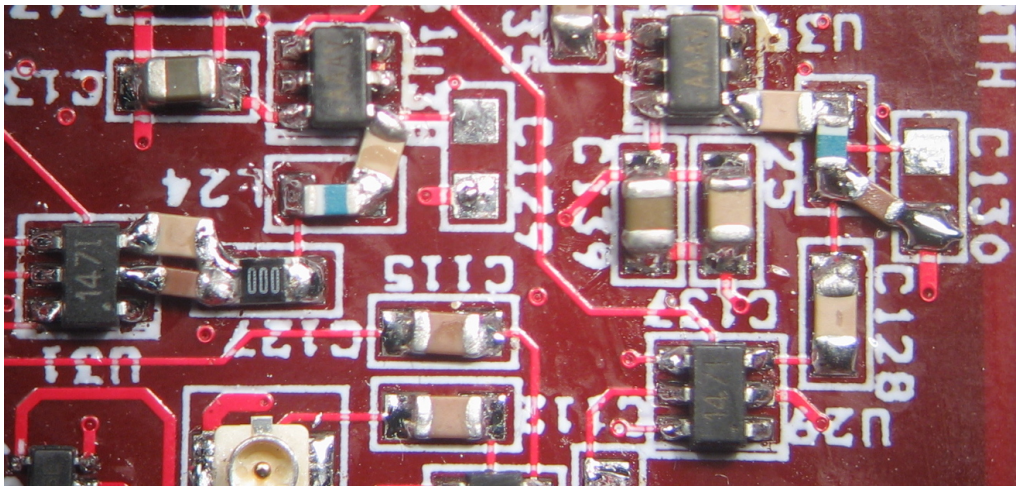


Figure 26: Parts placement for input matching network.

4.6.2 Output

As I stated earlier, soldering the output matching network is significantly easier thanks to an excess of pads. No traces need cutting or modification in any way.

1. Solder 8 pF capacitors on C135 and C131.
2. Install two 0 Ω resistors on L26 and L27.
3. Install two 12 nH inductors on C136 and C140.
4. Install two 4 pF capacitors on C138 and C141.

4.7 Sustainability and Societal Impacts

In terms of sustainability, this Senior Project will allow much lower power consumption at the Cal Poly Earth Station. Currently, a 100 watt amplifier, and 19 dB of antenna gain, is necessary to command the satellite. At only 25% efficient, the amplifier consumes nearly 400 watts of power during transmit. This low-noise amplifier circuit would eliminate the need for this amplifier, saving power and heating the atmosphere less.

The societal impacts include furthering the art of satellite communications. This may be the first time that the MAX2640 amplifier has flown in space, so we will see how well it performs. With an improved uplink capability, we will be able to do much more interesting tests with this satellite versus CP3, including taking some high-resolution pictures of the earth.

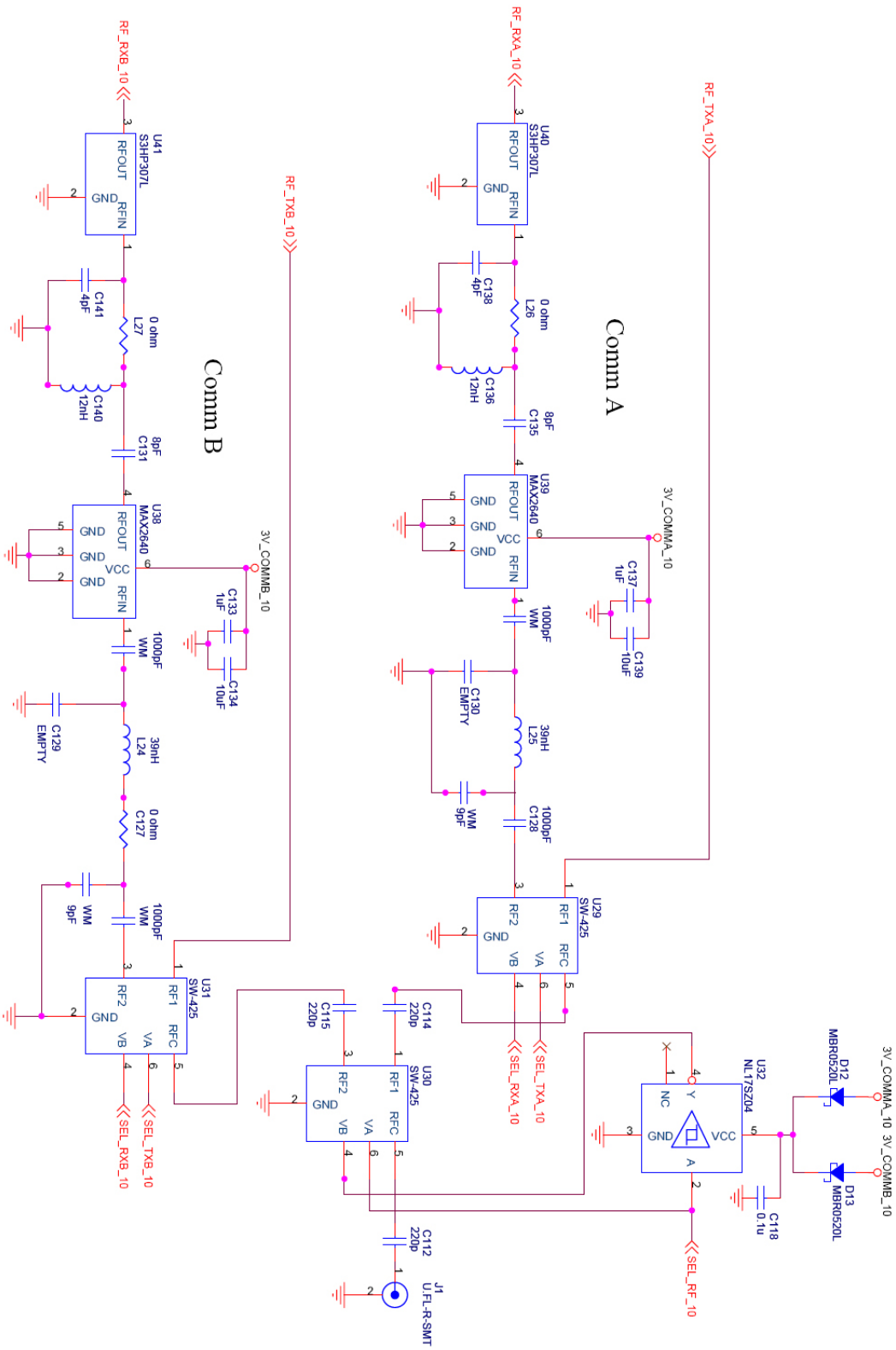


Figure 27: Final schematic with all part values. U29 and U31 are the TX/RX switches for each of the two communication subsystems, and U30 switches between Comm A and Comm B via one signal (SEL_RF_10) from the main C&DH processor. Wire mods are labelled WM.

5 Future Work

This project is far from done. Much more work is necessary before the spacecraft is ready to fly in space. With the launch scheduled for 19 October 2008, the PolySat team has just under two months to get everything ready. Some of the following items are necessary to complete before launch, but due to time constraints are not included in this report. Other items are more long-term, and may be completed before CP5 launches in the future.

5.1 Full System Testing

The entire receiver should be tested to ensure that these modifications did not accidentally decrease receive sensitivity in any way. This will require an extension of the completed tests to include the RF switches, as well as all the front panel RF circuitry, including the low-pass filter, balun, matching network, and antenna interface.

5.2 Range Tests

During the course of verifying that the LNA actually improved the receive sensitivity, the PolySat team performed some basic range testing of the new C&DH board versus the old C&DH board. The results showed a slight improvement, around 10 dB, but there were several problems with our testing procedures. I would like to perform these tests several more times, with the satellite several miles away from Cal Poly. I would also like to perform more bench testing using around 130 dB of attenuation to eliminate the effects of atmospheric distortion and multipath.

5.3 Internal Noise Characterization

The internal noise of the spacecraft has never been characterized. The three PIC processors, switching DC-DC converters, cameras, camera processor, and I^2C bus all use oscillators and switching circuits, generating noise when those components are on.

An easy way to see how much this internal noise effects the receiver includes putting the spacecraft into a Faraday cage with a spectrum analyzer connected to the receive pin on the CC1000, with a broad-band amplifier to increase the interference above the noise floor of the Spectrum Analyzer.

5.4 Addition of Shielding

Currently, there is no shielding around any of the RF electronics, allowing noise from any part of the spacecraft to easily enter the receiver. Adding a metal cover would be very easy, as the different RF sections are already segregated on the PCB. The ground plane under the RF sections could also be disconnected from the main spacecraft ground plane to further reduce noise.

5.5 Antenna Performance

Tiffany Lim's senior project[15] successfully used the Anechoic chamber to measure the radiation pattern of the spacecraft. However, the results were somewhat inconclusive, as

she only found one antenna null where there should be two nulls off the ends of the dipole antenna. More testing is necessary.

Due to the antenna route design, the current antenna is a little too short for 437 MHz. It is resonant at 468 MHz. The antenna needs to be lengthened, but this will require the antenna route to be redesigned, as well as the nichrome antenna deployment burner. Since we know our current design works in space, any modifications will need to be thoroughly tested in a vacuum chamber.

5.6 RF Module

The RF2117 RF power amplifier used in this design is no longer in production, and we have very limited quantities available for future satellites. A new amplifier chip will need to be added to the transceiver, and this new amplifier will require new matching to the board. Breaking the RF section off onto a separate board, completely independent from the main C&DH board with a standardized interface, would allow RF development to continue without affecting the circuits on the main C&DH PCB. Different modules, with different frequency bands and modulation schemes, could be installed in a short time.

6 Conclusion

This Senior Project successfully improved the receive sensitivity of the CPX Bus. I made the satellite more sensitive to ground transmissions by adding a Maxim MAX2640 low-noise amplifier and a Coilcraft S3HP307 high-pass filter to the receiver circuit of the CC1000 transceiver. The final circuit includes around 14.8 dB of gain with a 2.2 dB noise figure. Reverse isolation is around 44 dB with low input and output SWR.

Several engineering challenges prevented me from easily accomplishing this goal. The amplifier input is highly reflective, requiring many iterations of matching. The final circuit required modification of the printed circuit board. As with any new electronics destined for space, there are still many tests to perform on this circuit, such as total system performance, duration tests, and more temperature testing.

Fixing the communication subsystem of the CP3 satellite will allow the PolySat team to perform more tests and take more pictures with the satellite. Less RF power is needed on the ground to command the satellite, resulting in less power wasted on the ground and less atmospheric heating.

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A CP3 On-Orbit Data

This section contains on-orbit data from the CP3 spacecraft. The download occurred at 11:35 PDT on 14 May 2008 at the Cal Poly Earth Station, and the times on the graphs show the spacecraft's internal time. All of the data plots clearly display when the spacecraft entered eclipse, shown by the rapid decrease in temperature or voltage, and where the satellite enters the sun again.

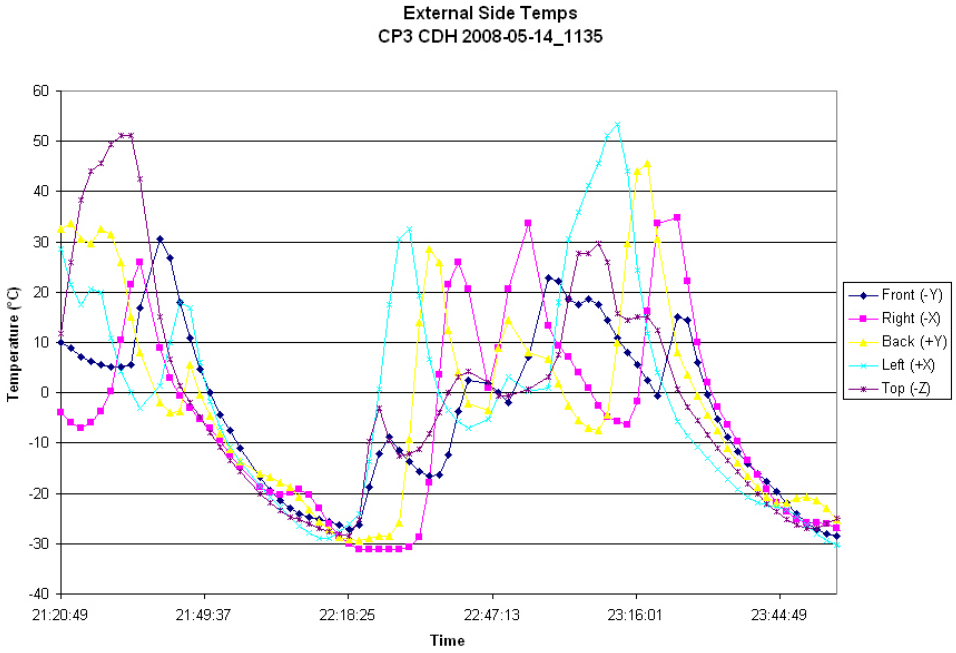


Figure 28: CP3 side panel external temperatures. Notice that it takes about 15 minutes after the satellite enters the sunlight before the Right (-X) side starts heating, indicating the rotation rate is very slow.

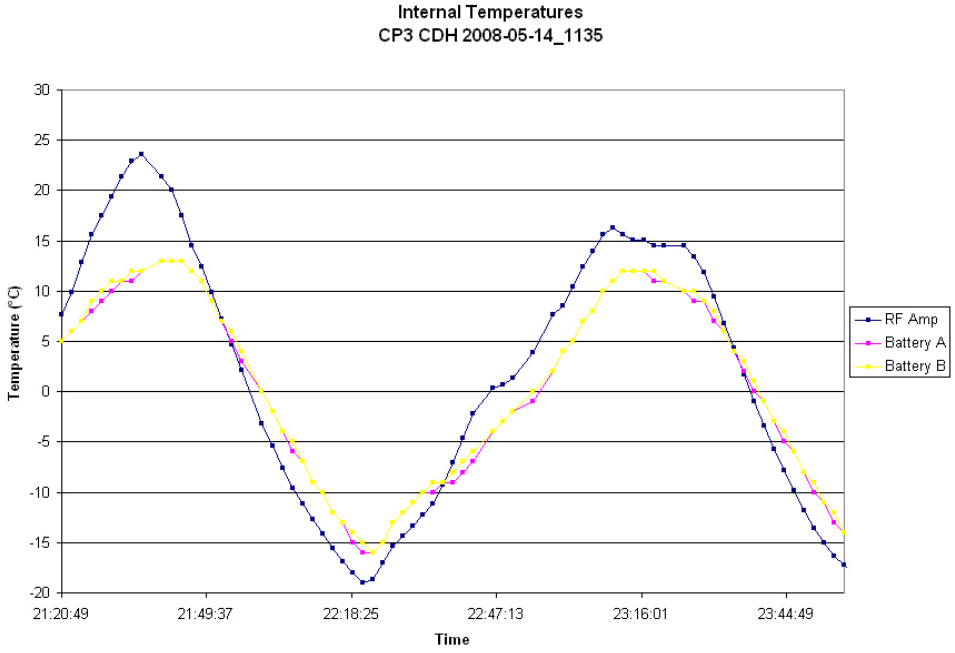


Figure 29: CP3 internal bus temperatures. The LNA is located very near to the RF Amp temperature sensor, and varies between –20℃ and +25℃.

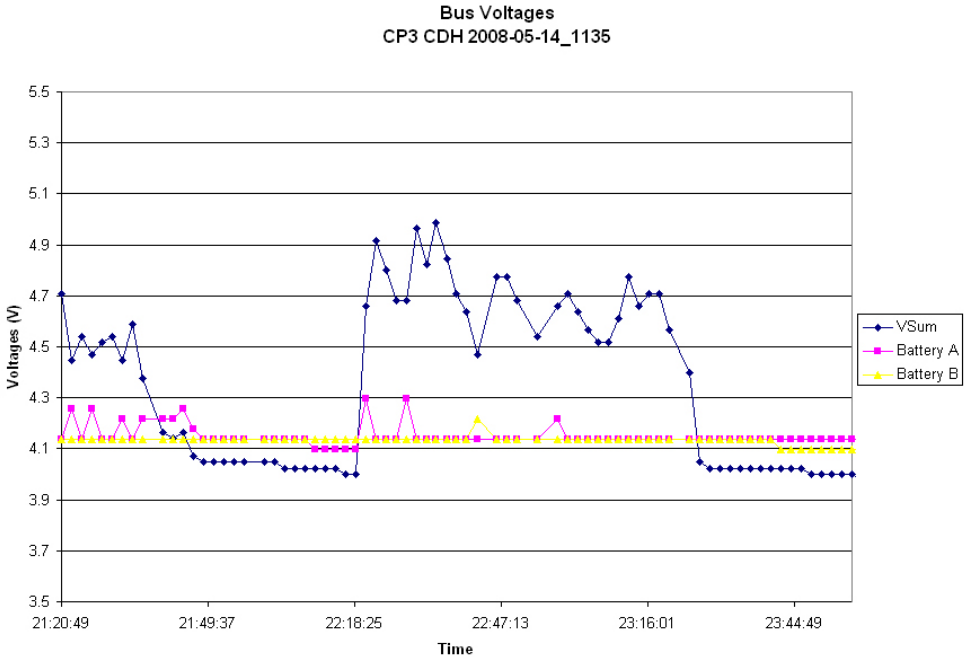


Figure 30: CP3 bus voltages. VSum is unregulated solar panel voltage. Notice that the batteries are never discharged, a result of our inability to tell the satellite to do anything to drain the batteries.

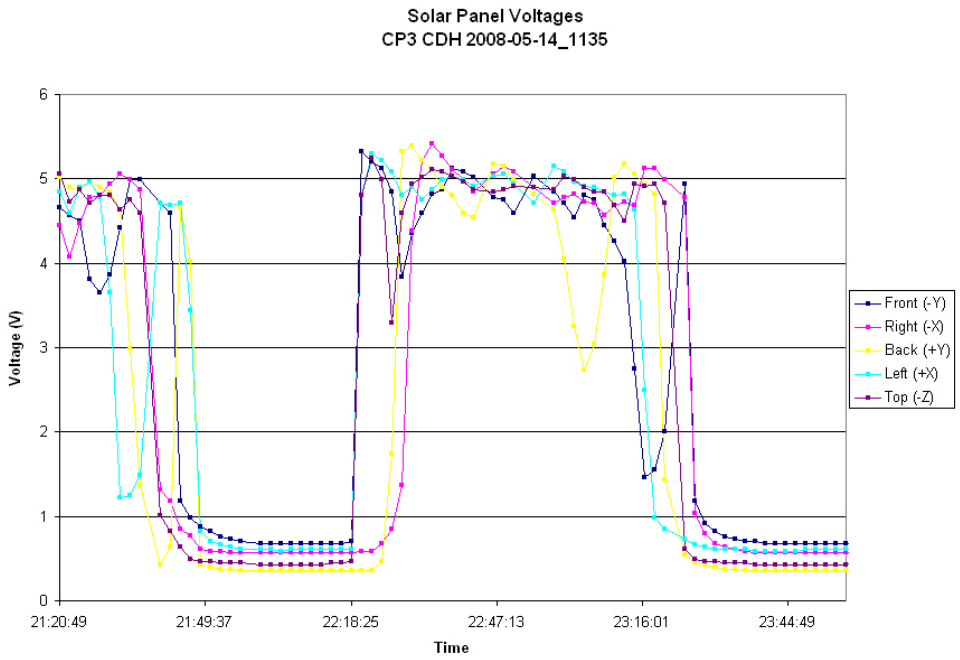


Figure 31: CP3 solar panel voltages. Because the satellite is not doing anything, the batteries are always full and the solar cells are always at their open-circuit voltage.

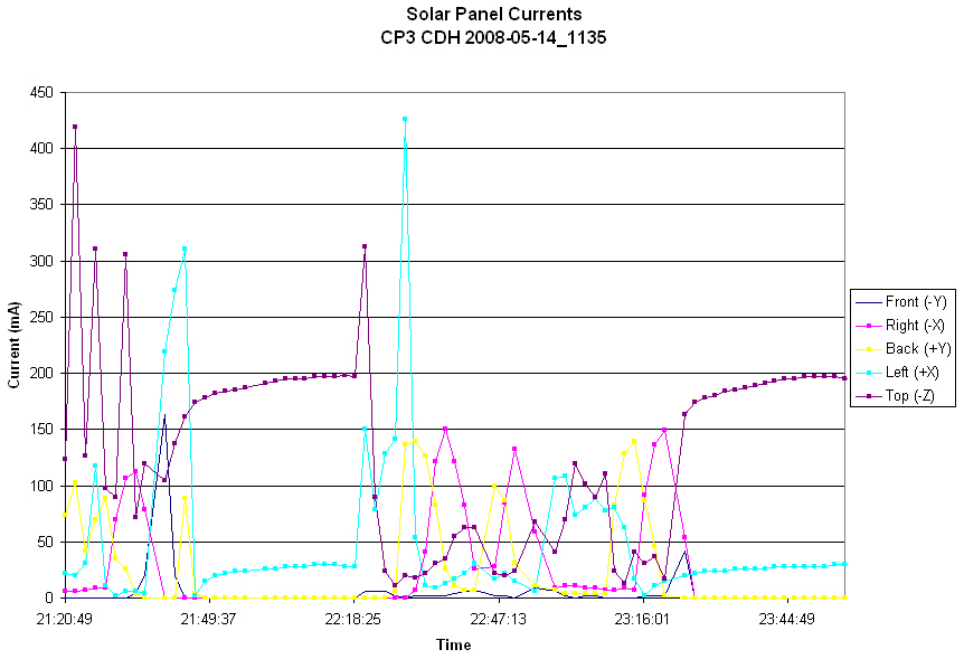


Figure 32: CP3 solar panel currents. Notice that the Top (-Z) panel shows around 200 mA during eclipse. A similar problem occurs on the Left (+X) side panel. These problems are due to mis-calibrated current sensors.

B Datasheets

B.1 Maxim MAX2640-2640 Low Noise Amplifier

B.2 Coilcraft S3HP307 High-Pass Filter

B.3 M/A-COM SW-425 RF Switch

19-1384; Rev 3; 4/07

EVALUATION KIT AVAILABLE

300MHz to 2500MHz SiGe Ultra-Low-Noise Amplifiers

General Description

The MAX2640/MAX2641 are low-cost, ultra-low-noise amplifiers designed for applications in the cellular, PCS, GPS, and 2.4GHz ISM frequency bands. Operating from a single +2.7V to +5.5V supply, these devices consume only 3.5mA of current while providing a low noise figure, high gain, high input IP3, and an operating frequency range that extends from 300MHz to 2500MHz.

The MAX2640 is optimized for 300MHz to 1500MHz applications, with a typical performance of 15.1dB gain, input IP3 of -10dBm, and a noise figure of 0.9dB at 900MHz. The MAX2641 is optimized for 1400MHz to 2500MHz applications, with a typical performance of 14.4dB gain, an input IP3 of -4dBm, and a noise figure of 1.3dB at 1900MHz.

These devices are internally biased, eliminating the need for external bias resistors and chokes. In a typical application, the only external components needed are a two-element input match, input and output blocking capacitors, and a V_{CC} bypass capacitor.

The MAX2640/MAX2641 are designed on a high-frequency, low-noise, advanced silicon-germanium process and are offered in the space-saving 6-pin SOT23 package.

Applications

315MHz/400MHz/900MHz/2.4GHz ISM Radios

Cellular/PCS Handsets

GPS Receivers

Cordless Phones

Wireless LANs

Wireless Data

Automotive RKE

Features

- **Wide Operating Frequency Range**
  - **MAX2640: 300MHz to 1500MHz**
  - **MAX2641: 1400MHz to 2500MHz**
- **Low Noise Figure**
  - **MAX2640: 0.9dB at 900MHz**
  - **MAX2641: 1.2dB at 1575MHz**
  - **1.3dB at 1900MHz**
  - **1.5dB at 2450MHz**
- **High Gain**
  - **MAX2640: 15.1dB at 900MHz**
  - **MAX2641: 15.7dB at 1575MHz**
  - **14.4dB at 1900MHz**
  - **13.5dB at 2450MHz**
- **High Reverse Isolation**
  - **MAX2640: 40dB at 900MHz**
  - **MAX2641: 31dB at 1575MHz**
  - **30dB at 1900MHz**
  - **24dB at 2450MHz**
- **+2.7V to +5.5V Single-Supply Operation**
- **Low 3.5mA Supply Current**
- **Ultra-Small SOT23-6 Package**

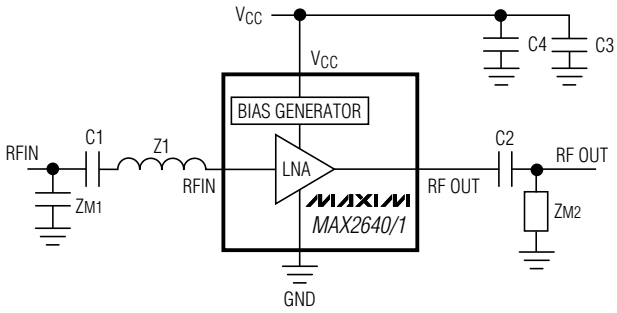
Ordering Information

PART	TEMP RANGE	PIN-PACKAGE	SOT TOP MARK
MAX2640EUT-T	-40°C to +85°C	6 SOT23-6	AAAV
MAX2640EUT+T	-40°C to +85°C	6 SOT23-6	AAAV
MAX2640AUT+T	-40°C to +125°C	6 SOT23-6	AAAV
MAX2641EUT-T	-40°C to +85°C	6 SOT23-6	AAAW
MAX2641EUT+T	-40°C to +125°C	6 SOT23-6	AAAW

+Indicates lead-free package.

Pin Configuration appears at end of data sheet.

Typical Operating Circuits



FREQUENCY (MHz)		C1 VALUE (pF)	C2 VALUE (pF)	C3 VALUE (pF)	C4 VALUE (pF)	Z1* VALUE (nH)	ZM1 VALUE (pF)	ZM2 VALUE
MAX2640	MAX2641							
900	—	470	3	470	—	9.85	2	—
—	1575	100	100	470	—	5.6	1	6.8nH
—	1900	470	100	470	—	2.55	1	1pF
—	2450	470	100	470	100	1.65	1	1pF

*The series inductor Z1 can be replaced by a transmission line of appropriate impedance and electrical length.

300MHz to 2500MHz SiGe Ultra-Low-Noise Amplifiers

ABSOLUTE MAXIMUM RATINGS

V_{CC} to GND .....-0.3V to +6V
RFIN Power (50Ω source) (Note 1) .....+5dBm
Continuous Power Dissipation (T_A = +70°C)
SOT23-6 (derate 8.7mW/°C above +70°C).....696mW

Operating Temperature Range
MAX2640EUT/MAX2641EUT .....-40°C to +85°C
MAX2640AUT .....-40°C to +125°C
Storage Temperature Range .....-65°C to +160°C
Lead Temperature (soldering, 10s) .....+300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Note 1: Pin must be AC-coupled with a DC blocking capacitor.

CAUTION! ESD SENSITIVE DEVICE

DC ELECTRICAL CHARACTERISTICS

(V_{CC} = +2.7V to +5.5V, T_A = -40°C to +85°C (MAX2640EUT/MAX2641EUT), T_A = -40°C to +125°C (MAX2640AUT), unless otherwise noted. Typical values are at V_{CC} = +3.0V, T_A = +25°C.) Limits at T_A = +25°C are guaranteed by production test. Limits over temperature are guaranteed by design and characterizarion.

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Operating Supply Voltage		2.7		5.5	V
Operating Supply Current	T_A = +25°C		3.5	4.7	mA
	T_A = -40°C to +85°C (MAX2640EUT/MAX2641EUT)			6.4	
	T_A = -40°C to +125°C (MAX2640AUT)			7.8	

RF ELECTRICAL CHARACTERISTICS

(V_{CC} = +3.0V, P_{RFIN} = -34dBm, Z_O = 50Ω, T_A = +25°C, unless otherwise noted.) (Notes 2 and 3)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
MAX2640 (f_{RFIN} = 900MHz)					
RFIN Frequency Range		300		1500	MHz
Gain		12.8	15.1		dB
Gain Variation Over Temperature	T_A = -40°C to +85°C (MAX2640EUT)		0.6	1.7	dB
	T_A = -40°C to +125°C (MAX2640AUT)		0.9	2.5	
Noise Figure	(Note 4)		0.9	1.1	dB
Input Return Loss			-11		dB
Output Return Loss			-14		dB
Reverse Isolation			40		dB
Input 1dB Gain Compression Point			-22		dBm
Input Third-Order Intercept Point	(Note 5)		-10		dBm
MAX2641 (f_{RFIN} = 1900MHz)					
RFIN Frequency Range		1400		2500	MHz
Gain		12.4	14.4		dB
Gain Variation Over Temperature	T_A = T_{MIN} to T_{MAX}		0.9	2.4	dB
Noise Figure	(Note 4)		1.3	1.5	dB
Input Return Loss			-12		dB
Output Return Loss			-12		dB
Reverse Isolation			30		dB
Input 1dB Gain Compression Point			-21		dBm
Input Third-Order Intercept Point	(Note 6)		-4		dBm

RF ELECTRICAL CHARACTERISTICS (continued)

(V_{CC} = +3.0V, P_{RFIN} = -34dBm, Z_O = 50Ω, T_A = +25°C, unless otherwise noted.) (Notes 2 and 3)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
MAX2641 (f_{RFIN} = 1575MHz)					
Gain			15.7		dB
Noise Figure	(Note 4)		1.2		dB
Input Return Loss			-8		dB
Output Return Loss			-15		dB
Reverse Isolation			-31		dB
Input 1dB Gain Compression Point			-21		dBm
Input Third-Order Intercept Point	(Note 7)		+1.4		dBm
MAX2641 (f_{RFIN} = 2450MHz)					
Gain			13.5		dB
Noise Figure	(Note 4)		1.5		dB
Input Return Loss			-10		dB
Output Return Loss			-11		dB
Reverse Isolation			-24		dB
Input 1dB Gain Compression Point			-19		dBm
Input Third-Order Intercept Point	(Note 8)		-2.5		dBm

Note 2: Guaranteed by design and characterization.

Note 3: Measured using typical operating circuit. Input and output impedance matching networks were optimized for best simultaneous gain and noise-figure performance.

Note 4: External component and circuit losses degrade noise-figure performance. Specification excludes external component and circuit board losses.

Note 5: Measured with two input tones, f_1 = 899MHz, f_2 = 901MHz, both at -34dBm per tone.

Note 6: Measured with two input tones, f_1 = 1899MHz, f_2 = 1901MHz, both at -34dBm per tone.

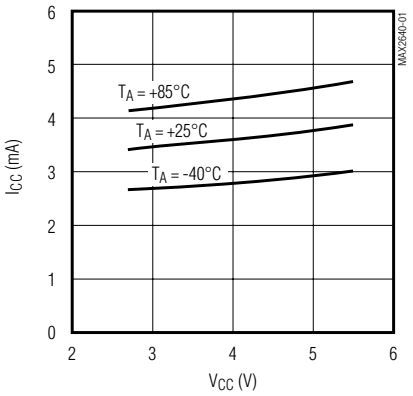
Note 7: Measured with two input tones, f_1 = 1574MHz, f_2 = 1576MHz, both at -34dBm per tone.

Note 8: Measured with two input tones, f_1 = 2449MHz, f_2 = 2451MHz, both at -34dBm per tone.

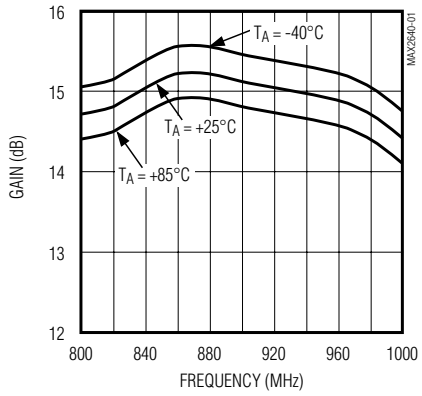
Typical Operating Characteristics

(V_{CC} = +3V, P_{RFIN} = -34dBm, Typical Operating Circuits, T_A = +25°C, unless otherwise noted.)

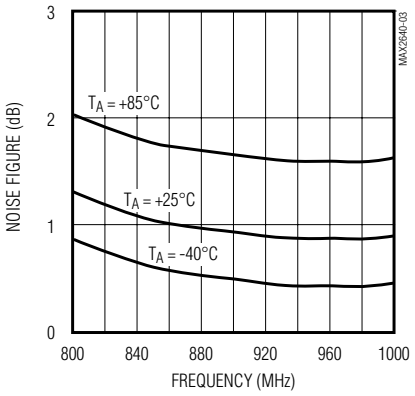
MAX2640
SUPPLY CURRENT vs. SUPPLY VOLTAGE



MAX2640 MATCHED AT 900MHz
GAIN vs. FREQUENCY



MAX2640 MATCHED AT 900MHz
NOISE FIGURE vs. FREQUENCY

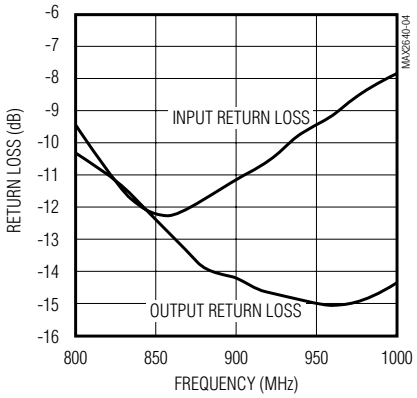


300MHz to 2500MHz SiGe Ultra-Low-Noise Amplifiers

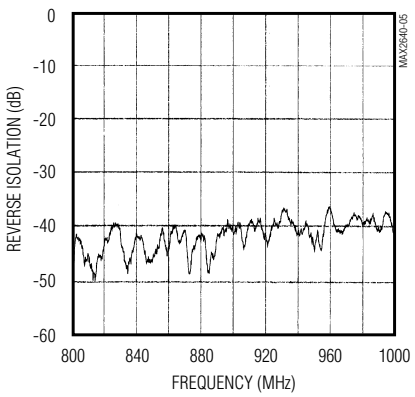
Typical Operating Characteristics (continued)

(V_{CC} = +3V, P_{RFIN} = -34dBm, Typical Operating Circuits, T_A = +25°C, unless otherwise noted.)

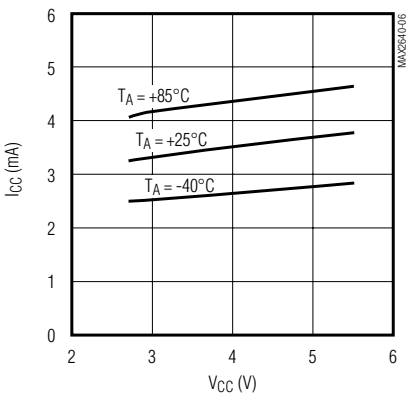
MAX2640 MATCHED AT 900MHz INPUT RETURN LOSS AND OUTPUT RETURN LOSS vs. FREQUENCY



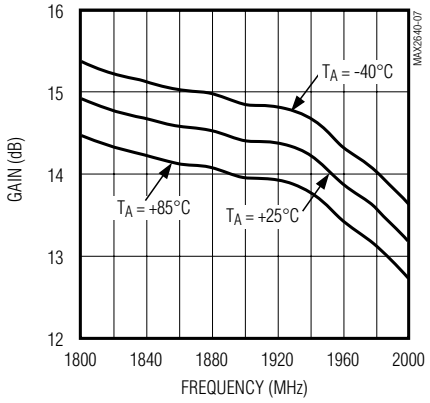
MAX2640 MATCHED AT 900MHz REVERSE ISOLATION vs. FREQUENCY



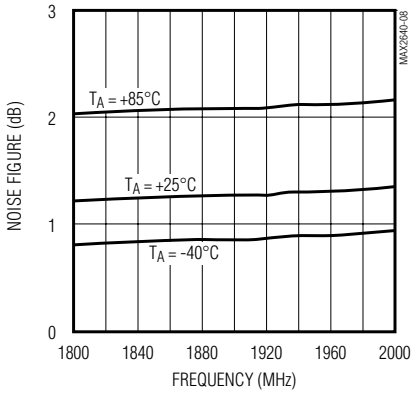
MAX2641 SUPPLY CURRENT vs. SUPPLY VOLTAGE



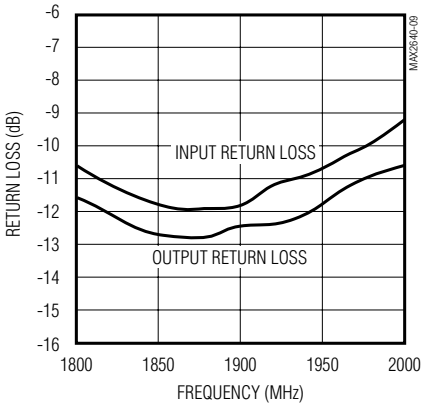
MAX2641 MATCHED AT 1900MHz GAIN vs. FREQUENCY



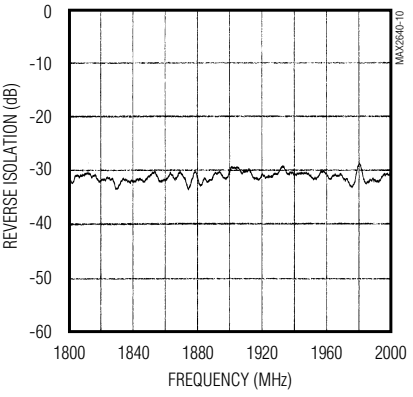
MAX2641 MATCHED AT 1900MHz NOISE FIGURE vs. FREQUENCY



MAX2641 MATCHED AT 1900MHz INPUT RETURN LOSS AND OUTPUT RETURN LOSS vs. FREQUENCY



MAX2641 MATCHED AT 1900MHz REVERSE ISOLATION vs. FREQUENCY



Pin Description

PIN	NAME	FUNCTION
1	RFIN	Amplifier Input. AC-couple to this pin with a DC blocking capacitor. Use recommended input matching network (see *Typical Operating Circuit*).
2, 3, 5	GND	Ground. For optimum performance, provide a low inductance connection to the ground plane.
4	RFOUT	Amplifier Output. Use the recommended series blocking or matching capacitor (see *Typical Operating Circuit*).
6	V_{CC}	Supply Voltage. Bypass to ground directly at the supply pin. The value of the bypass capacitor is determined by the lowest operating frequency. Additional bypassing may be necessary for long V_{CC} lines (see *Typical Operating Circuit*).

Detailed Description

The MAX2640 and MAX2641 are ultra-low-noise amplifiers that operate with RF input frequency ranges of 300MHz to 1500MHz (MAX2640) or 1400MHz to 2500MHz (MAX2641). These devices are available in SOT23-6 packages and contain internal bias circuitry to minimize the number of required external components. Their small size and low external component count make them ideal for applications where board space is limited.

Applications Information

External Matching Components

The MAX2640/MAX2641 are easy to use, generally requiring only five external components as shown in the *Typical Operating Circuit*. To reduce external component count further, replace external inductors with microstrip transmission lines. The high reverse isolation allows the tuning of the input matching network without affecting the output match, and vice versa. Select input and output matching networks to obtain the desired combination of gain, noise figure, and return loss performance. The *Typical Operating Circuits* show the recommended input and output matching networks for the MAX2640/MAX2641 at 900MHz and 1900MHz, respectively. These values are optimized for best simultaneous gain, noise figure, and return loss performance. To aid in the design of matching networks for other frequencies, Tables 1 and 2 list typical device S-parameters and Tables 3 and 4 list typical device noise parameters.

300MHz to 2500MHz SiGe Ultra-Low-Noise Amplifiers

Table 1. MAX2640 Typical Scattering Parameters at V_{CC} = +3V, T_A = +25°C

FREQUENCY (MHz)	S11 MAG	PHASE	S21 MAG	PHASE	S12 MAG	PHASE	S22 MAG	PHASE
400	0.907	-35.1	4.62	109.1	0.001	13.5	0.302	108.4
500	0.882	-43.1	4.70	90.4	0.001	64.7	0.33	93.6
600	0.858	-50.8	4.76	70.7	0.001	55.2	0.352	81.5
700	0.832	-58.1	4.80	50.6	0.002	39.4	0.365	69.4
800	0.810	-64.9	4.85	29.5	0.004	64.2	0.384	56.8
900	0.788	-71.0	4.77	9.2	0.005	36.3	0.396	44.7
1000	0.771	-76.6	4.74	-12.0	0.007	28.0	0.412	33.5
1100	0.749	-82.3	4.55	-32.4	0.010	12.3	0.436	21.9
1200	0.735	-88.0	4.48	-53.4	0.013	-10.6	0.455	10.7
1300	0.720	-93.4	4.24	-75.9	0.015	-28.2	0.469	-0.2
1400	0.702	-98.8	4.17	-94.9	0.021	-42.9	0.482	-9.9
1500	0.688	-104.9	3.81	-117.5	0.024	-59.8	0.489	-20.2

Table 2. MAX2641 Typical Scattering Parameters at V_{CC} = +3V, T_A = +25°C

FREQUENCY (MHz)	S11 MAG	PHASE	S21 MAG	PHASE	S12 MAG	PHASE	S22 MAG	PHASE
1500	0.734	-75.5	4.397	-90.5	0.013	-80.3	0.535	17.7
1600	0.717	-80.3	4.209	-109.8	0.016	-91.9	0.514	8.6
1700	0.695	-85.3	4.193	-131.6	0.018	-116.5	0.513	-0.5
1800	0.678	-90.6	3.876	-150.0	0.021	-128.7	0.510	-10.6
1900	0.661	-96.6	3.801	-173.5	0.023	-150.6	0.493	-21.6
2000	0.646	-102.6	3.456	166.9	0.026	-166.6	0.470	-32.0
2100	0.632	-108.8	3.302	146.4	0.028	171.7	0.431	-43.4
2200	0.620	-114.0	2.981	123.6	0.029	150.7	0.403	-56.1
2300	0.610	-119.4	2.781	105.3	0.033	132.2	0.374	-69.4
2400	0.604	-124.6	2.430	82.9	0.032	111.2	0.338	-86.2
2500	0.603	-128.4	2.118	64.7	0.030	95.7	0.316	-98.3

Table 3. MAX2640 Typical Noise Parameters at V_{CC} = +3V, T_A = +25°C

FREQUENCY (MHz)	f_{MIN} (dB)	$\lvert\Gamma_{opt}\rvert$	Γ_{opt} ANGLE	R_N (Ω)
400	0.66	0.56	21	12.5
500	0.69	0.54	25	11.9
600	0.72	0.51	30	11.3
700	0.75	0.48	35	10.8
800	0.78	0.46	40	10.2
900	0.82	0.43	45	9.7
1000	0.85	0.40	50	9.3
1100	0.89	0.37	56	8.8
1200	0.93	0.35	62	8.3
1300	0.97	0.32	68	7.9
1400	1.01	0.29	77	7.4
1500	1.06	0.26	84	7.0

Table 4. MAX2641 Typical Noise Parameters at V_{CC} = +3V, T_A = +25°C

FREQUENCY (MHz)	f_{MIN} (dB)	$\lvert\Gamma_{opt}\rvert$	Γ_{opt} ANGLE	R_N (Ω)
1500	1.02	0.43	44	12.4
1600	1.05	0.40	47	11.8
1700	1.08	0.38	50	11.3
1800	1.10	0.36	54	10.8
1900	1.14	0.32	58	10.3
2000	1.17	0.30	62	9.9
2100	1.20	0.28	66	9.4
2200	1.23	0.25	71	9.0
2300	1.27	0.22	77	8.6
2400	1.30	0.19	82	8.3
2500	1.34	0.17	91	8.0

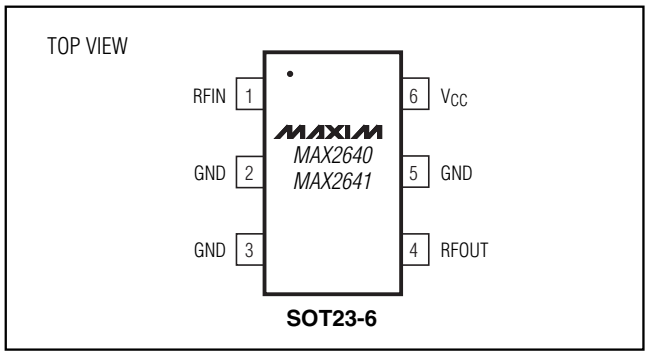
Layout and Power-Supply Bypassing

A properly designed PC board is essential to any RF/microwave circuit. Be sure to use controlled impedance lines on all high-frequency inputs and outputs. The power supply should be bypassed with decoupling capacitors located close to the device V_{CC} pins. For long V_{CC} lines, it may be necessary to add additional decoupling capacitors. These additional capacitors can be located further away from the device package.

Proper grounding of the GND pins is essential. If the PC board uses a topside RF ground, connect it directly to all GND pins. For a board where the ground plane is not on the component side, the best technique is to connect the GND pin to the board with a plated through-hole close to the package.

300MHz to 2500MHz SiGe Ultra-Low-Noise Amplifiers

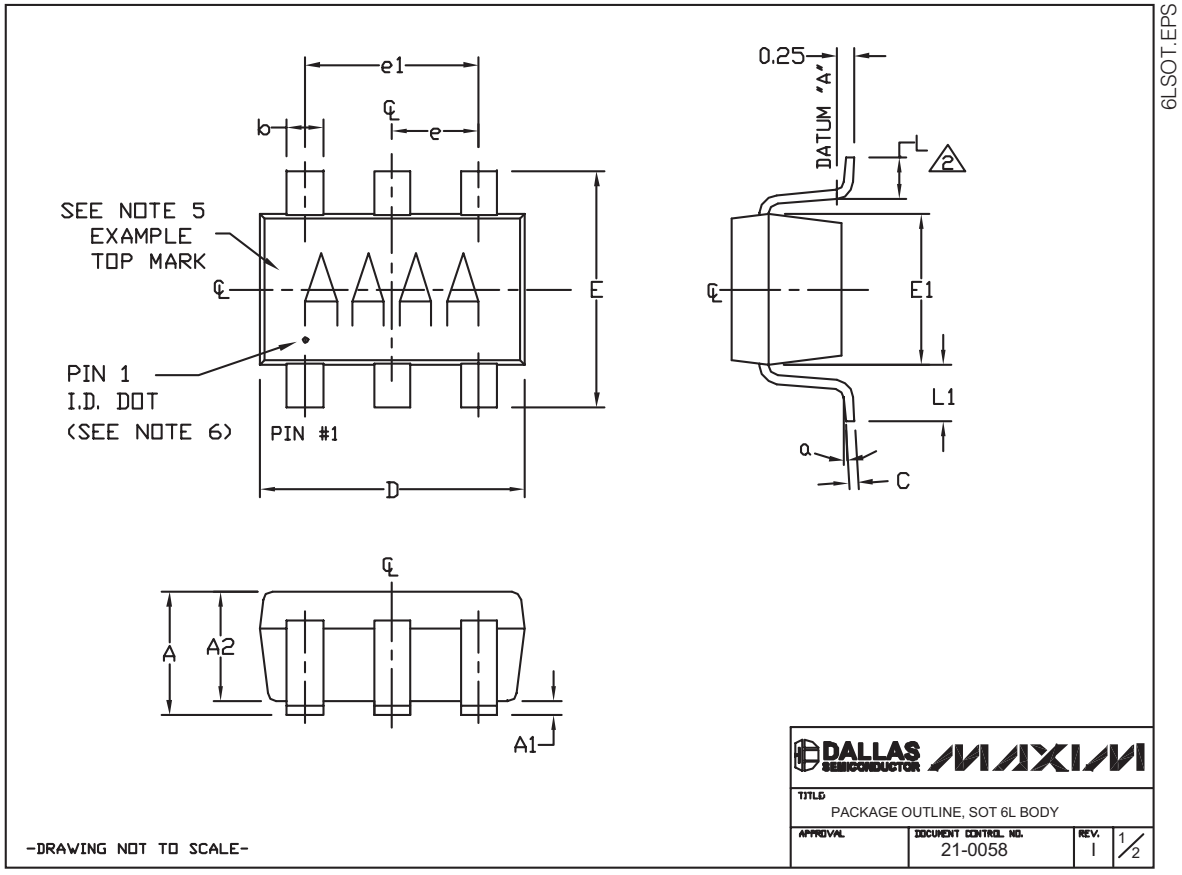
Pin Configuration



SOT23-6

Package Information

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information, go to **www.maxim-ic.com/packages**.)



Package Information (continued)

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information, go to **www.maxim-ic.com/packages**.)

NOTES:

1. ALL DIMENSIONS ARE IN MILLIMETERS.
2. FOOT LENGTH MEASURED AT INTERCEPT POINT BETWEEN DATUM A & LEAD SURFACE.
3. PACKAGE OUTLINE EXCLUSIVE OF MOLD FLASH & METAL BURR. MOLD FLASH, PROTRUSION OR METAL BURR SHOULD NOT EXCEED 0.25mm.
4. PACKAGE OUTLINE INCLUSIVE OF SOLDER PLATING.
5. PIN 1 IS LOWER LEFT PIN WHEN READING TOP MARK FROM LEFT TO RIGHT. (SEE EXAMPLE TOP MARK)
6. PIN 1 I.D. DOT IS 0.3mm ø MIN. LOCATED ABOVE PIN 1.
7. MEETS JEDEC MO178, VARIATION AB.
8. SOLDER THICKNESS MEASURED AT FLAT SECTION OF LEAD BETWEEN 0.08mm AND 0.15mm FROM LEADTIP.
9. LEAD TO BE COPLANAR WITHIN 0.1mm.
10. NUMBER OF LEADS SHOWN ARE FOR REFERENCE ONLY.
11. MARKING IS FOR PACKAGE ORIENTATION REFERENCE ONLY.

SYMBOL	MIN	NOMINAL	MAX
A	0.90	1.25	1.45
A1	0.00	0.05	0.15
A2	0.90	1.10	1.30
b	0.35	0.40	0.50
C	0.08	0.15	0.20
D	2.80	2.90	3.00
E	2.60	2.80	3.00
E1	1.50	1.625	1.75
L	0.35	0.45	0.60
L1		0.60 REF.	
e1		1.90 BSC.	
e		0.95 BSC.	
α	0°	2.5°	10°

PKG CODES:
U6-1, U6-2, U6-4, U6C-8,
U6SN-1, U6CN-2, U6S-3, U6F-5,
U6F-6, U6FH-5, U6FH-6

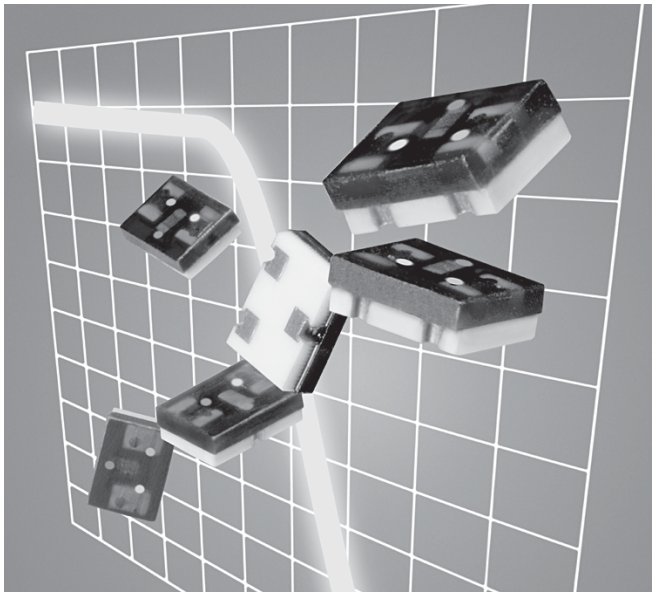
-DRAWING NOT TO SCALE-

DALLAS SEMICONDUCTOR MAXIM

TITLE: PACKAGE OUTLINE, SOT 6L BODY

APPROVAL	DOCUMENT CONTROL NO.	REV.	
	21-0058	I	2/2

Surface Mount LC Filters



These space saving low and high pass filters are pre-tuned, tight tolerance modules which serve a wide variety of filtering requirements.

They feature 3rd order Butterworth alignment, less than 0.3 dB insertion loss and a compact, 1812-size construction ideally suited for auto insertion and reflow soldering.

- 3rd order Butterworth alignment
- 50 Ohm characteristic impedance
- Less than 0.3 dB insertion loss

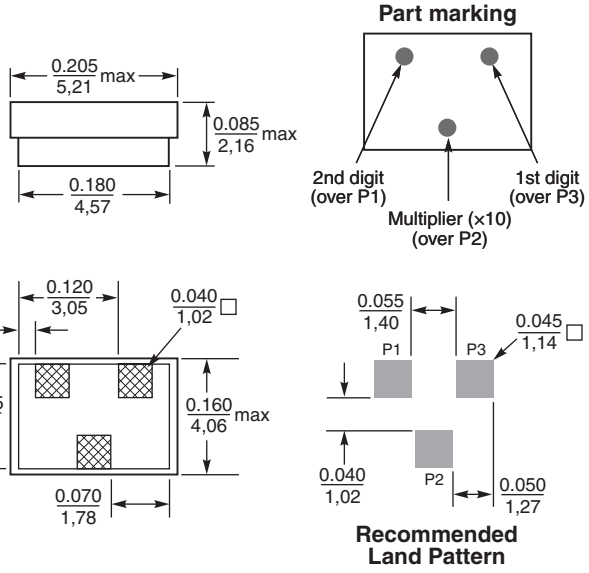
Coilcraft **Designer's Kit D302** contains samples of all low pass filters. To order, contact Coilcraft or visit **http://order.coilcraft.com**.

Low Pass Filters

Part number[1]	-3 dB Cutoff	Irms (mA)[2]
S3LP156L_	15 MHz	200
S3LP306L_	30 MHz	300
S3LP606L_	60 MHz	300
S3LP157L_	150 MHz	400
S3LP307L_	300 MHz	400
S3LP507L_	500 MHz	500
S3LP707L_	700 MHz	500
S3LP807L_	800 MHz	500
S3LP907L_	900 MHz	500
S3LP108L_	1.0 GHz	500
S3LP128L_	1.2 GHz	500
S3LP158L_	1.5 GHz	500
S3LP188L_	1.8 GHz	500
S3LP218L_	2.1 GHz	500

High Pass Filters

Part number[1]	-3 dB Cutoff	Irms (mA)[2]
S3HP156L_	15 MHz	300
S3HP306L_	30 MHz	300
S3HP606L_	60 MHz	300
S3HP157L_	150 MHz	300
S3HP307L_	300 MHz	300
S3HP507L_	500 MHz	500
S3HP807L_	800 MHz	500



Weight: 64.7 – 69.0 mg
Tape and reel: 600/7″ reel; 2200/13″ reel 12 mm tape width
See Tape and Reel Specifications section for packaging data.
See Color Coding section for part marking data.

1. When ordering, please specify **termination** and **packaging** codes:

S3HP156L C

Termination: **L** = RoHS compliant silver over copper or gold over nickel over silver.
Special order: **T** = RoHS tin-silver-copper (95.5/4/0.5) or **S** = non-RoHS tin-lead (63/37).

Packaging: **C** = 7″ machine-ready reel. EIA-481 embossed plastic tape (600 parts per full reel).
B = Less than full reel. In tape, but not machine ready. To have a leader and trailer added ($25 charge), use code letter C instead.
D = 13″ machine-ready reel. EIA-481 embossed plastic tape (2200 parts per full reel).

2. Average current for a 15°C rise above 25°C ambient.
3. Operating temperature range -40°C to +85°C.
4. Electrical specifications at 25°C.

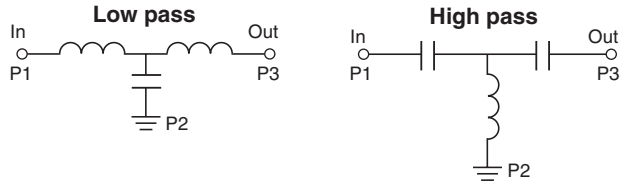
Coilcraft®

Specifications subject to change without notice.
Please check our website for latest information. Document 124-1 Revised 11/16/06

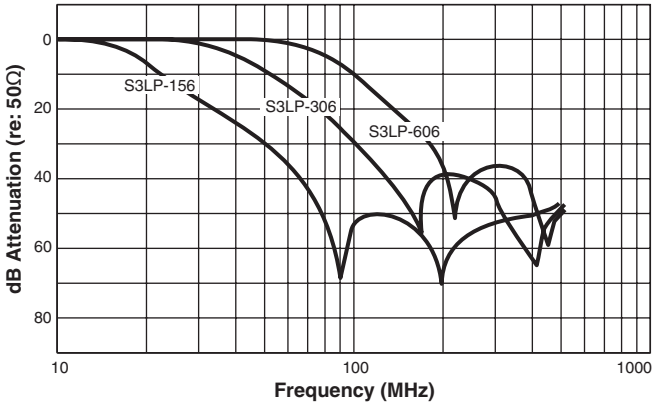
1102 Silver Lake Road Cary, Illinois 60013 **Phone** 847/639-6400 **Fax** 847/639-1469
E-mail info@coilcraft.com **Web** http://www.coilcraft.com

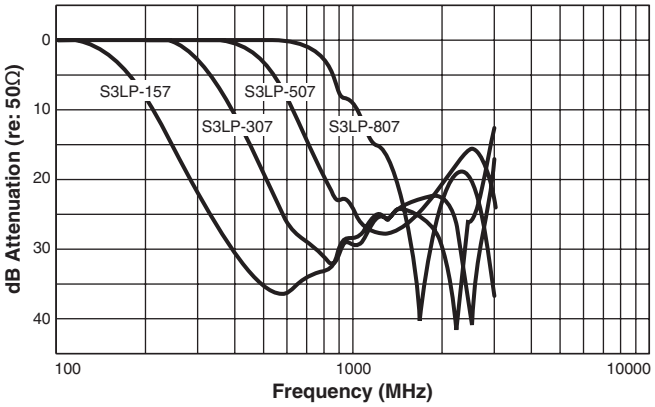
Surface Mount LC Filters

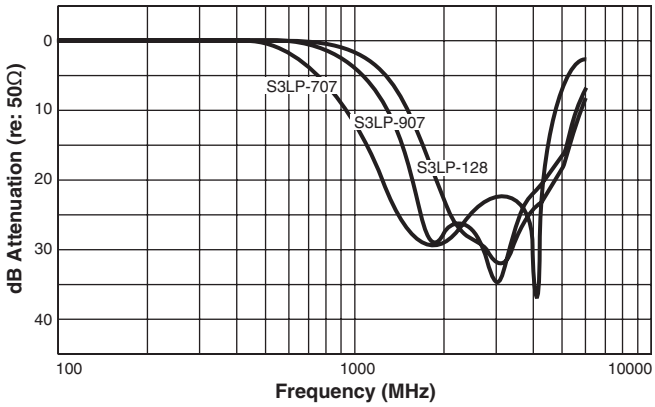
S-Parameter files
ON OUR WEB SITE OR CD

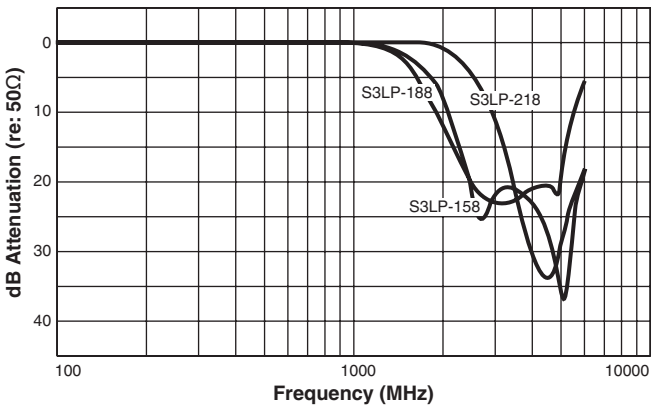


Frequency Response—Low Pass Filters*

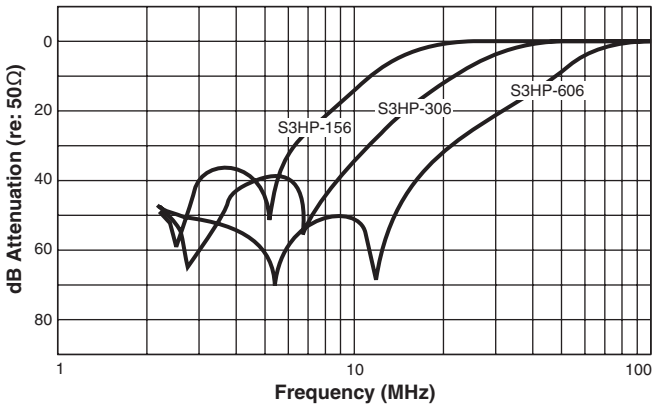


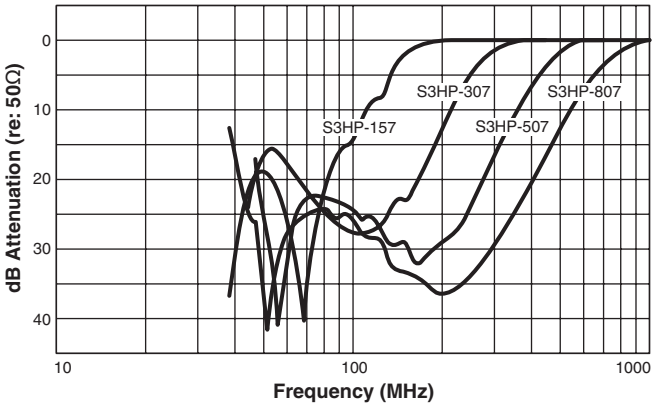






Frequency Response—High Pass Filters*





*Measured on Agilent/HP 8753D network analyzer

1102 Silver Lake Road Cary, Illinois 60013 **Phone** 847/639-6400 **Fax** 847/639-1469
E-mail info@coilcraft.com **Web** http://www.coilcraft.com

3 Watt Cellular T/R and Antenna Changeover Switch DC - 3.0 GHz

SW-425
V4

Features

- Low Cost Plastic SOT-26 Package
- Low Insertion Loss: < 0.6 dB @ 1900 MHz
- Low Power Consumption: <20µA @ +3V
- Very High Intercept Point: 53 dBm IP3
- Both Positive and Negative 2.5 to 8 V Control
- For CDMA, W-CDMA, TDMA, GSM, PCS and DCS Applications

Description

M/A-COM's SW-425 is a GaAs monolithic switch in a low cost SOT-26 surface mount plastic package. The SW-425 is ideally suited for applications where very low power consumption (<10µA@5V), low intermodulation products and very small size are required. Typical applications include Internal/External antenna select switch for portable telephones and data radios. In addition, because of its low loss, good isolation and inherent speed, the SW-425 can be used as a conventional T/R switch or as an antenna diversity switch. The SW-425 can be used in power applications up to 3 watts in systems such as cellular PCS, CDMA, W-CDMA, TDMA, GSM and other analog/digital wireless communications systems.

The SW-425 is fabricated using M/A-COM's 0.5 micron gate length GaAs PHEMT process. The process features full chip passivation for increased performance and reliability.

Ordering Information

Part Number	Package
SW-425 PIN	Bulk Packaging
SW-425TR	1000 piece reel

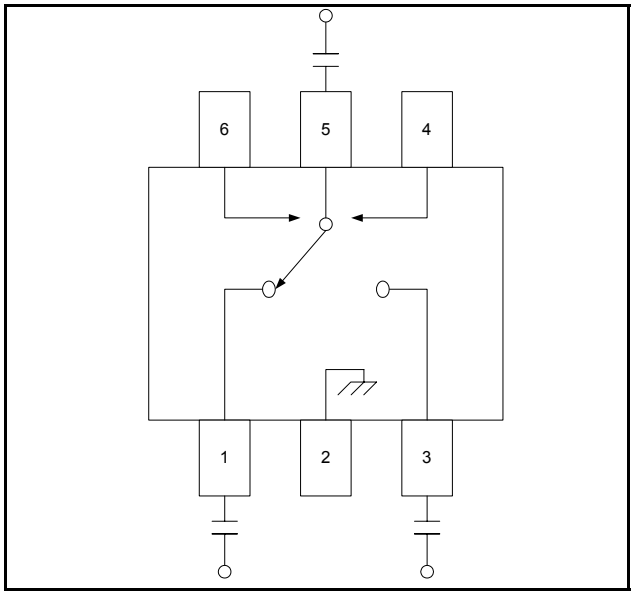
Note: Reference Application Note M513 for reel size information.

Absolute Maximum Ratings [1]

Parameter	Absolute Maximum
Input Power (0.5—3.0 GHz) 3 V Control 5 V Control	 +36 dBm +38 dBm
Operating Temperature	-40°C to +85°C
Storage Temperature	-65°C to +150°C

1. Exceeding any one or combination of these limits may cause permanent damage to this device.

Functional Diagram



Pin Configuration

Pin No.	Function	Pin No.	Function
1	RF1	4	VB
2	Ground	5	RF Common
3	RF2	6	VA

Truth Table

Mode (Control)	Control A	Control B	RFC - RF1	RFC - RF2
Positive[2]	0 ± 0.2 V +2.5 to +8 V	+2.5 to +8 V 0 ± 0.2 V	Off On	On Off
Positive/ Negative [2,3]	-Vc ± 0.2 V +Vc	+Vc -Vc ± 0.2 V	Off On	On Off
Negative[4]	0 ± 0.2 V -2.5 to -8 V	-2.5 to -8 V 0 ± 0.2 V	On Off	Off On

2. External DC blocking capacitors are required on all RF ports. 39 pF capacitors can be used for positive control voltage.
3. $[-V_{CTL}]$, $V_{CTL} \leq 8$ V
4. If negative control is used, DC blocking capacitors are not required on RF ports.

- **North America** Tel: 800.366.2266 / Fax: 978.366.2266
- **Europe** Tel: 44.1908.574.200 / Fax: 44.1908.574.300
- **Asia/Pacific** Tel: 81.44.844.8296 / Fax: 81.44.844.8298

Visit www.macom.com for additional data sheets and product information.

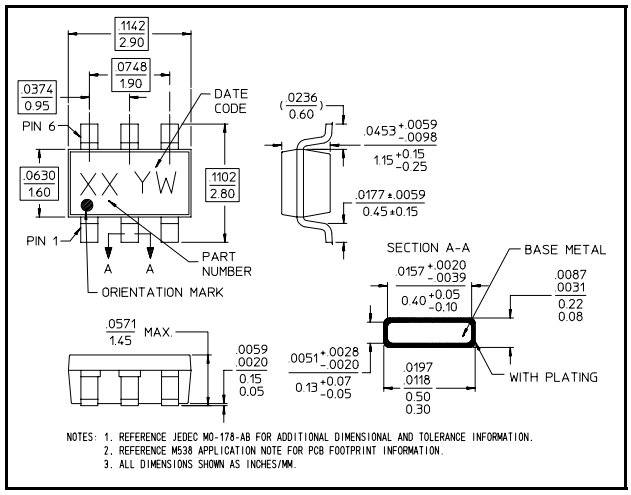
3 Watt Cellular T/R and Antenna Changeover Switch DC - 3.0 GHz

SW-425
V4

Electrical Specifications: T_A = +25°C

Parameter	Test Conditions	Units	Min	Typ	Max
Insertion Loss	DC - 1 GHz 1 - 2 GHz 2 - 3 GHz	dB dB dB	— — —	0.4 0.55 0.7	0.5 0.65 0.8
Isolation	DC - 1 GHz 1 - 2 GHz 2 - 3 GHz	dB dB dB	18 13 10	20 15 12	— — —
VSWR	DC - 3 GHz	Ratio	—	1.2:1	1.4:1
P1dB (3 V supply)	500 MHz - 3 GHz	dBm	32	34	—
P1dB (5 V supply)	500 MHz - 3 GHz	dBm	34	36	—
Input IP2	Two-Tone, 5 MHz spacing, +10 dBm (+13 dBm total) V_{CTL} = 3 V 0.9 GHz	dBm	62	70	—
Input IP3	Two-Tone, 5 MHz spacing, +10 dBm (+13 dBm total) V_{CTL} = 3 V 0.9 GHz	dBm	48	53	—
2nd Harmonics	Pin 30 dBm [V_{CTL}] = 3 V Pin 33 dBm [V_{CTL}] = 5 V	dBc dBc	65 65	70 75	— —
3rd Harmonics	Pin 30 dBm [V_{CTL}] = 3 V Pin 33 dBm [V_{CTL}] = 5 V	dBc dBc	45 65	48 75	— —
Trise, Tfall	10% to 90% RF, 90% to 10% RF	ns	—	60	—
Ton, Toff	50% Control to 90% RF, Control to 10% RF	ns	—	20	—
Transients	In-Band	mV	—	20	—
Gate Leakage Current	V_{CTL} = 3 V	µA	—	10	20

SOT-26



Handling Procedures

Please observe the following precautions to avoid damage:

Static Sensitivity

Gallium Arsenide Integrated Circuits are sensitive to electrostatic discharge (ESD) and can be damaged by static electricity. Proper ESD control techniques should be used when handling these devices.

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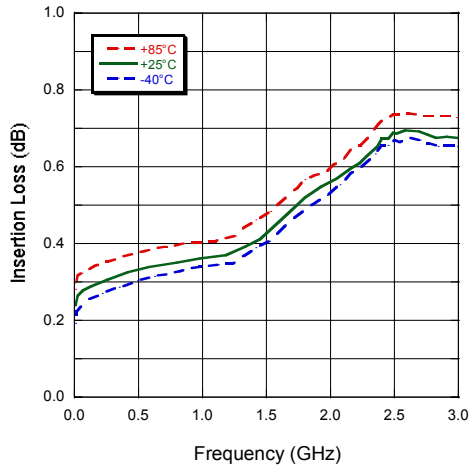
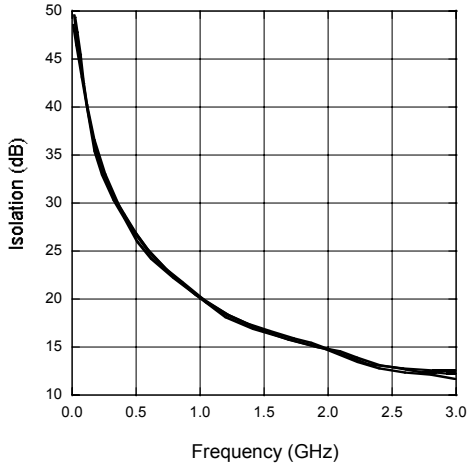
Typical Performance Curves

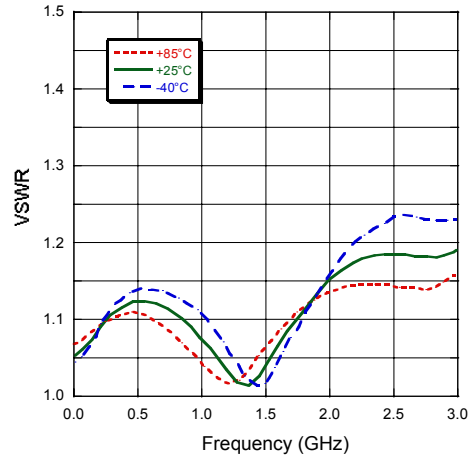
Insertion Loss



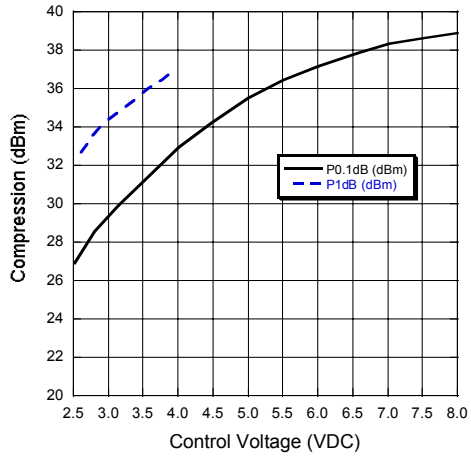
Isolation



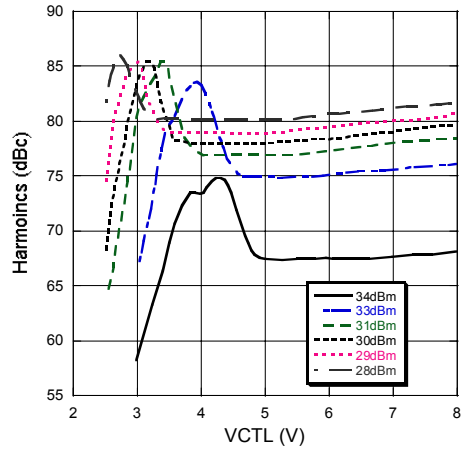
VSWR



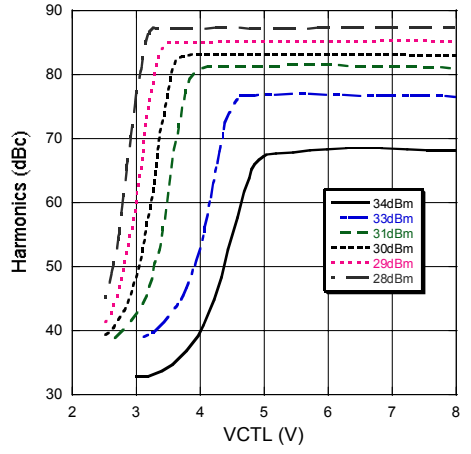
Input Compression Point vs. V_{CTL} @ 900 MHz



2nd Harmonic vs. V_{CTL} @ = 900 MHz



3rd Harmonic vs. V_{CTL} @ = 900 MHz



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