Improving Receive Sensitivity of the CPX Bus

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1 Introduction

Upon the successful launch of the CP2 and CP3 spacecraft in April 2007, the PolySat team immediately noticed a problem with the spacecraft's uplink margin. While the Cal Poly Earth Station could hear the satellites just fine, the satellites could not hear the earth station very well. It appears that the uplink problem relates to poor satellite receive sensitivity; however, as recent tests done at SRI International show, pass-dependent factors such as the orientation of the spacecraft might affect the link margin more than receive sensitivity.

Derek Huerta designed and built the communication subsystem for both satellites as part of his Masters Thesis in Spring 2006[1]. If everything went according to plan, CP2 would launch first and verify the communications subsystem. PolySat project members, who built the satellite, would fix the circuit before the next launch if it performs poorly in orbit. However, due to several delays and a launch failure[2], we made no improvements to the communications subsystem from CP2 to CP3.

This senior project will try and correct this situation. Scheduled to launch in June 2008, CP6 must function as well as possible, requiring an improved communications subsystem. To increase the uplink margin of the link, I will add a low noise amplifier (LNA) and a high-pass filter (HPF) just before the CC1000 receiver. The satellite's Front Panel already contains a low-pass filter (LPF).

2 Scope of Project

In order to increase the sensitivity of the satellite, I will add a LNA to the CPX bus[3]. The "CPX bus" refers to the next version of satellite containing all subsystems (power, structure, data storage, communications, etc) of our cubesat except the payload. Figure 1 shows the entire CPX communication subsystem, and Figure 2 shows the individual com-

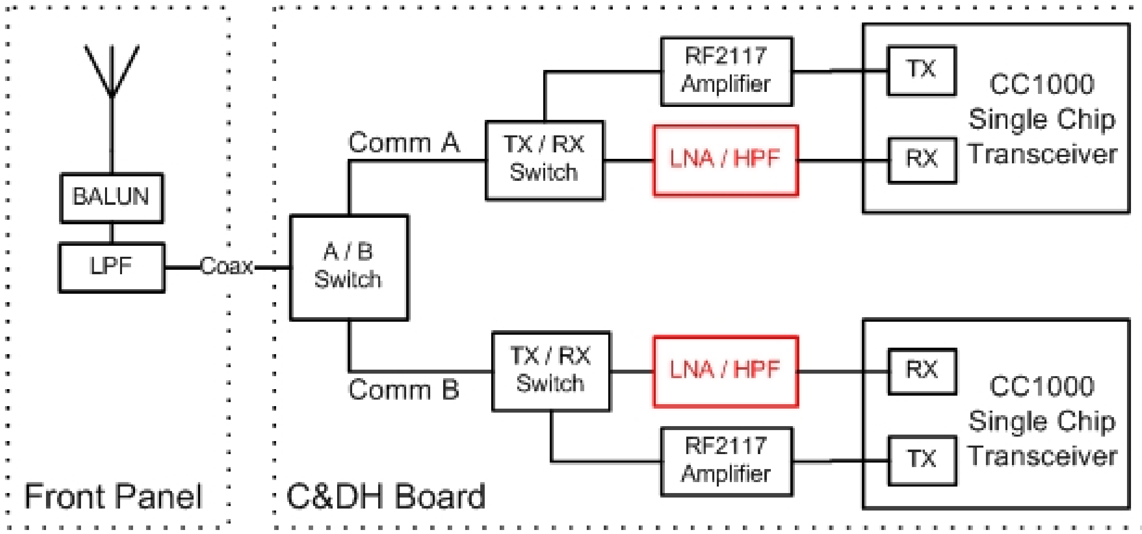

Figure 1: Block diagram of the satellite communications subsystem. Components not shown include the Comm A and Comm B processors, which control the A/B and TX/RX switches, RF2117 start-up sequence, and CC1000 single chip transceivers. This senior project resides within the LNA/HPF block, see Figure 2.

ponents of my senior project. As one can see, the scope of this project mostly encompasses matching the different devices to the 50 Ω characteristic impedance of the microstrip on the 6-layer FR4 PCB.

To make the matching process easier, I will purchase a development kit for the LNA. Based on the development kit, I will incorporate a rough matching network into the layout for the Command and Data Handling (C&DH) boards. This ensures the boards will not need fabrication again once I find the final matching network values.

Once I optimally match the LNA to the rest of the circuit, I will test the receive sensitivity. We never thoroughly tested the receive sensitivity of the original circuit, so the receive sensitivity of the old boards will be tested and compared to the new circuit. I will use the RF lab in Building 20 for this testing.

I will also test internal spacecraft noise to ensure none of the three processors on board create interference inside our satellite. These tests will show if spacecraft noise seriously

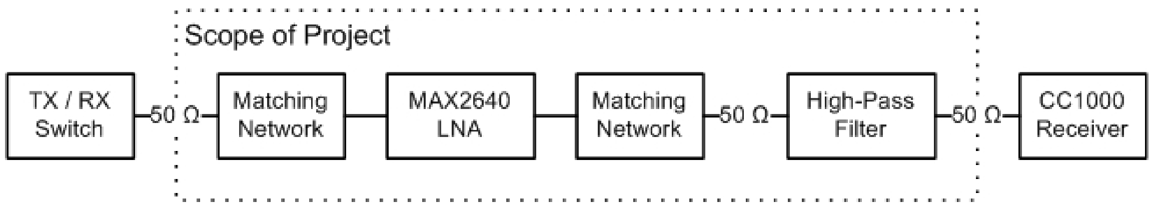

Figure 2: Scope of this senior project.

desensitizes our receiver; we never tested the spacecraft noise, and no shielding exists over any parts of the communication subsystem (including CC1000 single-chip transceiver). Also, to characterize antenna patterns possibly affecting the link margin, Tiffany Lim's Senior Project[4] on characterizing Cubesat antenna patters will extend in scope to include contained (undeployed) and partially deployed antennas.

3 Specification

In terms of size and weight, the final circuit must surface-mount and fit on the current C&DH board in the "empty spaces." While CP3's mass is about 813 grams, much less than the maximum 1 kg, anything to keep mass low would help the future payloads of the CPX bus. Figure 3 shows possible placements for the LNA and HPF.

In terms of power, less power consumed would help with the very slim (but positive) power budget. Two sources can power the chip: V_{COMM} provides a steady (but very noisy) 3.3 volts from the communications subsystem DC-DC converter, and V_{SUM} furnishes a noiseless 3.2 to 4.6 volts directly from the solar panels. V_{SUM} varies based on the amount of sunlight present and state of charge of the batteries[3].

Since every dB counts when it comes to receive sensitivity, the circuit should have as little loss as possible, especially before the LNA. In reality, I will aim for a 3 dB maximum mismatch loss figure, even though 3 dB equals half of the signal. More signal lost through the high-pass filter and CC1000 matching network is preferable because this loss occurs

Table 1: Project Specification.

Parameter	Value	Conditions
Maximum mass	20 grams	
Input voltages	3.3 or 3.2 to 4.6 volts	
Maximum filter loss	3 dB	437 MHz
Minimum LNA gain	10 dB	437 MHz
Maximum matching network loss	3 dB	437 MHz
Maximum LNA noise figure	2 dB	

after the LNA. Additionally, the noise figure of the LNA should be very low, less than 2 dB if possible. Table 1 shows the complete design specifications.

4 Schedule

I expect this project to take around 7 months. As one can seen on Gantt chart in Figure 4, this project started in the beginning of September 2007. Work has steadily progressed since then, but we have run into problems during electrical testing of the board. Several shorts exist in the PCB near the Umbilical Connector, shown in the very upper right of Figure 3. While we can wire-mod around these shorts, this requires extra time.

I will have help from other people in the Polysat lab for various tasks, including kitting, soldering, and testing the completed C&DH board. Since kitting, soldering, and testing a single C&DH board takes about 15 hours, I appreciate this extra help. Building a fully working power board also takes about 10 hours, and I will need at least one power board for this project. I will also have help from other Polysat personnel when time comes for the range tests.

5 Material List

The two major components of this design include a LNA and HPF. Other components required include various surface-mount ceramic capacitors and wound chip inductors for

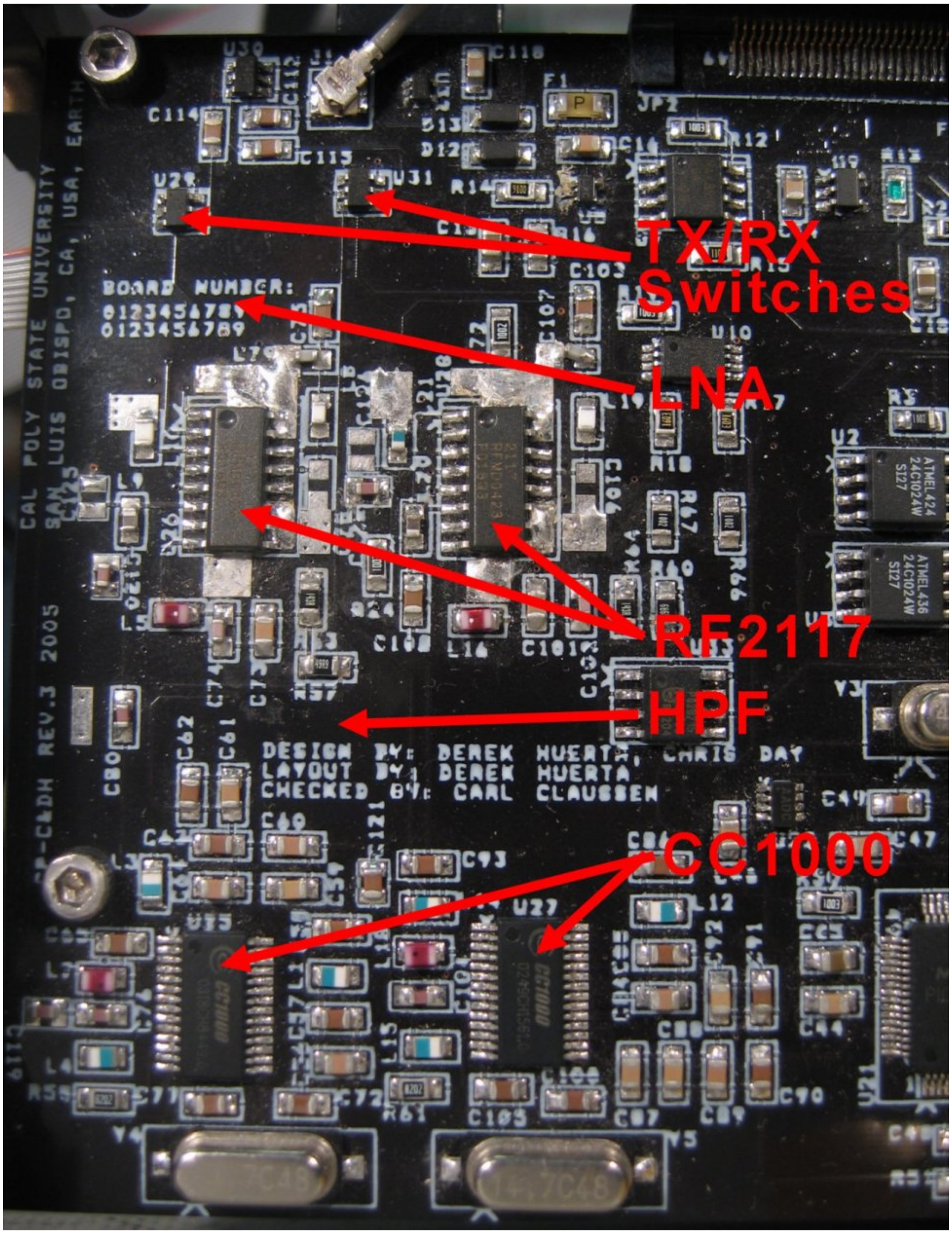

Figure 3: Original CP3 C&DH board. Markings show the important components of the circuit, as well as possible placement for the LNA and HPF. The coax at the top leads to the front panel, where the dipole antenna and balun reside.

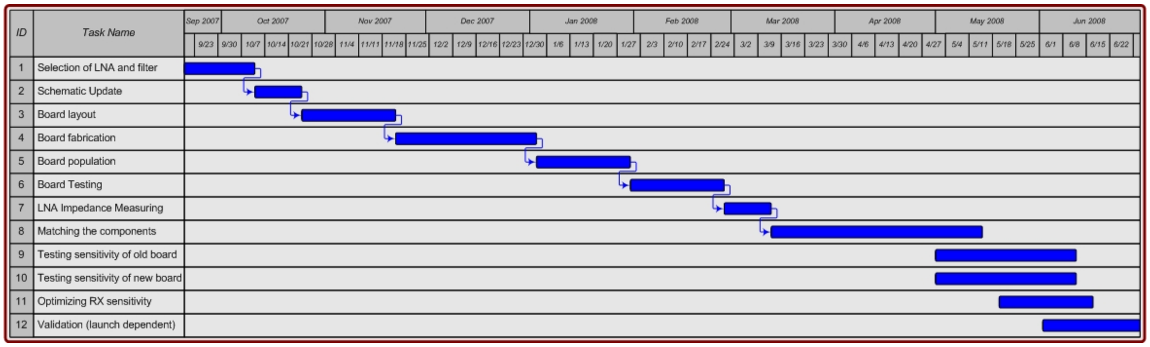

Figure 4: Project Timeline.

Table 2: Bill of materials.

Ref ID	Part	Description	Supplier
U39, U39	MAX2640	Low noise amplifier	Maxim IC
U40, U41	S3HP307L	High-pass filter	Coilcraft
C137, C139, C133, C134		LNA bypass capacitors	Digikey
C128, L25		Comm A LNA input network	Digikey
C127, L24		Comm B LNA input network	Digikey
C138, C136, L26		Comm A LNA output network	Digikey
C141, C140, L27		Comm B LNA output network	Digikey
C135, C131		LNA output blocking capacitors	Digikey

the matching networks. Refer to Table 2 for a complete bill of materials.

I had several options while selecting the LNA. I looked at several chips from Maxim IC, including the MAX2650 and MAX2633. I also looked at RF Micro Devices chips SGL-0163 and SPF-5043, and Analog Devices chips AD8353 and AD8354. Looking at the specifications in Section 3, I settled on the Maxim MAX2640. I used a similar process for selecting the HPF.

6 Major Risk Items

Aside from the obvious "this may catch fire," there are several risks to this senior project. Some of the risks include not correctly matching the components to the board, accidentally decreasing the receive sensitivity, and not finishing the project on time.

A slight possibility exists the LNA selected will not match to the board, or the required component values for matching cannot be purchased commercially. Along these same lines, a different type of matching network (such as a T network instead of a Pi network) would require fabrication of a new board. Building a new board could take up to four weeks, and would seriously jeopardize the timeline presented in Section 4.

Another risk to this project includes that my modifications to the C&DH board would actually decrease the sensitivity of the receiver. While very unlikely, a possible reason for this may lie in the manufacturing process of the boards. Since the boards for the satellites currently in space were made more than two years ago, different manufacturing processes might have changed the electrical characteristics of the board in a way we might not know about until the boards return from fabrication. All matching networks on the board would require modification, a large task.

References

[1] Huera, Derek. "Development of a Highly Integrated Communication System for use in Low Power Space Applications." Cal Poly Masters Thesis. April 2006.

[2] "The Dnepr Launcher." http://www.russianspaceweb.com/dnepr_007_belka.html. Accessed 21 Jan 2008.

[3] Day, Chris. "The Design of an Efficient, Elegant, and Cubic Pico-Satellite Electronics System." Cal Poly Masters Thesis. December 2004.

[4] Lim, Tiffany. "Antenna Characteristics of the Cubesat Dipole Antenna." Cal Poly Senior Project. July 2007.